九齊科技股份有限公司
Nyquest Technology Co., Ltd.

DATA SHEET

N25Q Series

Serial Flash with Quad SPI

Version 1.4

Aug. 10, 2022

Revision History

Version	Date	Description	Modified Page
1.0	2017/11/30	Formal release.	-
1.1	2020/03/13	Remove 64Mb and 128Mb parts.	-
1.2	2022/04/26	● Add erase/program cycles and retention period. ● Revise into N25Q016B & N25Q032C due to EOL.	3, 4, 13
1.3	2022/07/13	● Add tables / figures for status registers 1 & 2.	8, 9, 10, 11
1.4	2022/08/10	● Add Fast Read Dual I/O command (1-2-2) information. ● Add condition for V_{DD}.	3, 4, 7 14

1. 概述

N25Q 系列是九齊搭配微控制器或語音產品的高容量快閃記憶體。本系列支援標準序列周邊介面 (SPI) 及高速的兩線式輸出 / 雙向通訊 (Dual Output, Dual I/O)、四線式雙向通訊 (Quad I/O)。讀取模式下位址可以自動遞增以支援高效能的在地執行程式(XIP) 功能。

所有元件均以小體積的 SOP-150mil 封裝以節省空間。

2. 功能

- 寬廣的工作電壓：
  - 2.7V ~ 3.6V @ FR=104MHz / fR=50MHz。
  - 2.35V (min.) @ fR=32MHz
  - 2.15V (min.) @ fR=16MHz
- 資料寫入以 256-Byte (page) 為單位。
- 所有位址均支援小區塊清除指令 4K-Byte Sector、64K-Byte Block。
- 讀取模式下均有位址自動遞增功能。
- 每顆元件都有唯一識別碼，可作為保密功能。
- 一般讀取工作電流 9mA，省電模式電流 2uA。
- 高效能寫入及清除速度
  - 資料寫入時間 Page Program: 500us
  - 小區塊清除時間 Sector Erase:50ms typical
- 高效能串列式快閃記憶體
  - 抹除/寫入次數：100,000。
  - 資料保存時間：20年。
- 支援各種 SPI 通訊方式 (1-1-1, 1-1-2, 1-2-2, 1-4-4)

全系列詳細產品編號、容量及封裝方式表列如下：

產品編號	容量 (bit)	容量 (bit)	容量 (Byte)	容量 (Byte)	ID / JEDEC (HEX)	封裝
N25Q004A	4Mb	4,096Kb	0.5MB	512KB	12h / 13h	SOP8-150mil
N25Q008A	8Mb	8,192Kb	1MB	1,024KB	13h / 14h	SOP8-150mil
N25Q016B	16Mb	16,384Kb	2MB	2,048KB	14h / 15h	SOP8-150mil
N25Q032C	32Mb	32,768Kb	4MB	4,096KB	15h / 16h	SOP8-150mil

1. GENERAL DESCRIPTION

The N25Q series are High-Density Flash memory storage devices for Nyquest MCU or Voice IC product. This series supports standard Serial Peripheral Interface (SPI), and also two-bit (Dual Output, Dual I/O) and four bit (Quad I/O) protocols for higher performance. The Continues Read Modes allow for efficient memory access as XIP (execute in place) operation.

All devices are offered in space-saving packages for SOP-150mil.

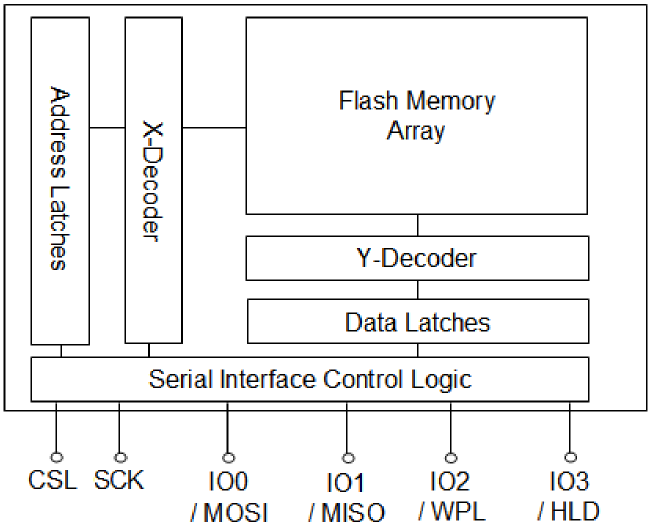
2. FEATURES

- Wide operating voltage range:
  - 2.7V ~ 3.6V @ F_R=104MHz / f_R=50MHz。
  - 2.35V (min.) @ f_R=32MHz
  - 2.15V (min.) @ f_R=16MHz
- 256-Byte per programmable page.
- Uniform 4K-Byte Sectors, 64K-Byte Blocks.
- Auto-increment Read capability.
- 64-bit Unique ID for each device as a security option.
- 9mA typical active current, 2uA typical power down current.
- High performance program/erase speed
  - Page Program time: 500us
  - Sector Erase time: 50ms typical
- High performance Serial Flash
  - More than 100,000 erase/program cycles
  - More than 20-year data retention
- Supports SPI command in 1-1-1, 1-1-2, 1-2-2, and 1-4-4 modes.

Detail Part Number, Flash Memory size, and Package are listed in the following table.

P/N	Flash Size (bit)	Flash Size (bit)	Flash Size (Byte)	Flash Size (Byte)	ID / JEDEC (HEX)	Package
N25Q004A	4Mb	4,096Kb	0.5MB	512KB	12h / 13h	SOP8-150mil
N25Q008A	8Mb	8,192Kb	1MB	1,024KB	13h / 14h	SOP8-150mil
N25Q016B	16Mb	16,384Kb	2MB	2,048KB	14h / 15h	SOP8-150mil
N25Q032C	32Mb	32,768Kb	4MB	4,096KB	15h / 16h	SOP8-150mil

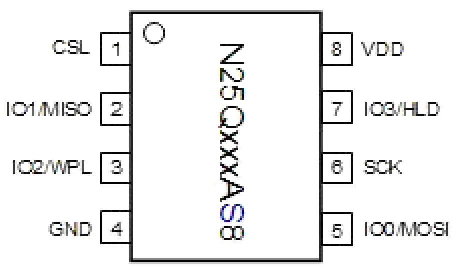
3. BLOCK DIAGRAM



4. PIN ASSIGNMENT

N25Q series provides the same package type for all parts: SOP8, 150mil.

SOP8, 150 mil



5. PIN DESCRIPTION

Pin Name	ATTR.	Description
VDD	Power	Positive power.
GND	Power	Negative power.
CSL	Input	Chip Select, active Low.
SCK	Input	Serial Clock Input.
IO0 / MOSI	I/O	IO0 for Quad mode. Master out Slave in for SPI mode.
IO1 / MISO	I/O	IO1 for Quad mode. Master in Slave out for SPI mode.
IO2 / WPL	I/O	IO2 for Quad mode. Write Protect Input for SPI mode, active Low.
IO3 / HLD	I/O	IO3 for Quad mode. Hold Input for SPI mode, active Low.

6. I/O PORTS

6.1 CSL (Chip Select)

The SPI Chip Select (CSL) pin enables and disables device operation. When CSL is high the device is deselected and the all Data Output pins (MISO or IO0, IO1, IO2, IO3) are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or status register cycle is in progress. When CSL is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, CSL must transition from high to low before a new instruction will be accepted.

6.2 SCK (Serial Clock Input)

The SPI Serial Clock Input (SCK) pin provides the timing for serial input and output operations.

6.3 IO0 / MOSI

The MOSI (Master Out Slave In) pin is used to transfer data serially into the device in SPI mode. It receives instructions, address and data to be programmed. Data is latched on the rising edge of the SCK (Serial Clock) input pin. The MOSI pin becomes IO0 - an input and output during Dual and Quad commands for receiving instructions, address, and data to be programmed (values latched on rising edge of SCK) as well as shifting out data (on the falling edge of SCK).

6.4 IO1 / MISO

The MISO (Master In Slave Out) pin is used to transfer data serially out of the device in SPI mode. Data is shifted out on the falling edge of the SCK (Serial Clock) input pin. MISO becomes IO1 - an input and output during Dual and Quad commands for receiving instructions, addresses, and data to be programmed (values latched on rising edge of SCK) as well as shifting out data (on the falling edge of SCK).

6.5 IO2 / WPL

The WPL (Write Protect) pin can be used to prevent the Status Register from being written. The WPL function is not available when the Quad mode is enabled. The WPL function is replaced by IO2 for input and output during Quad mode for receiving addresses and data to be programmed (values are latched on rising edge of the SCK) as well as shifting out data (on the falling edge of SCK).

6.6 IO3 / HLD

The HLD pin allows the device to be paused while it is actively selected. When HLD is brought low, while CSL is low, the MISO pin will be at high impedance and signals on the MOSI and SCK pins will be ignored (don't care). When HLD is brought high, device operation can resume. The HLD function is replaced by IO3 for input and output during Quad mode for receiving addresses and data to be programmed (values are latched on rising edge of the SCK) as well as shifting out data (on the falling edge of SCK).

7. INSTRUCTIONS

	Instruction					
Command Name	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
RDSR-1	05h	SR1 [7:0]				
RDSR-2	35h	SR2 [7:0]				
WREN	06h					
EWSR	50h					
WRDI	04h					
WRST-1	01h	SR1 [7:0]				
WRSR-2	31h	SR2 [7:0]				
Page Program	02h	A23-A16	A15-A8	A7-A0	D7-D0	
Sector Erase (4 KB)	20h	A23-A16	A15-A8	A7-A0		
Block Erase (64 KB)	D8h	A23-A16	A15-A8	A7-A0		
Chip Erase	C7h					
Enable Reset	66h					
Reset Device	99h					
Read Data	03h	A23-A16	A15-A8	A7-A0	(D7-D0,…)	
Fast Read	0Bh	A23-A16	A15-A8	A7-A0	dummy	(D7-D0,…)
Fast Read Dual Output	3Bh	A23-A16	A15-A8	A7-A0	dummy	(D7-D0,…)(1)
Fast Read Dual I/O	BBh	A23-A8(2)	A7-A0, M7-M0	(D7-D0,…)		
Fast Read Quad I/O	EBh	A23-A0,M7-M0(3)	(x,x,x,x,D7-D0,...)(4)	(D7-D0,…)		
Deep Power-down	B9h					
Release Power down	ABh	dummy	dummy	dummy	ID	
Device ID	90h	dummy	dummy	00h	20h	ID
JEDEC ID	9Fh	20h	40h	JEDEC		
Read Unique ID	4Bh	dummy	dummy	dummy	dummy	(UID63-0)

Notes:

1. Dual Output data

   IO0 = (D6, D4, D2, D0)

   IO1 = (D7, D5, D3, D1)

2. Dual Input Address

   IO0 = A22, A20, A18, A16, A14, A12, A10, A8 A6, A4, A2, A0, M6, M4, M2, M0

   IO1 = A23, A21, A19, A17, A15, A13, A11, A9 A7, A5, A3, A1, M7, M5, M3, M1

3. Quad Input Address

   IO0 = A20, A16, A12, A8, A4, A0, M4, M0

   IO1 = A21, A17, A13, A9, A5, A1, M5, M1

   IO2 = A22, A18, A14, A10, A6, A2, M6, M2

   IO3 = A23, A19, A15, A11, A7, A3, M7, M3

4. Quad Output Data

   IO0 = (D4, D0, …..)

IO1 = (D5, D1, …..)

IO2 = (D6, D2, …..)

IO3 = (D7, D3, …..)

8. Status Registers

8.1 N25Q004A

Table 8.1 Status Register-1 (SR1)

Bits	Field	Function	Type	Default State	Description
7	SRP0	Status Register Protect 0	Non-volatile and Volatile versions	0	0 = WP# input has no effect or Power Supply Lock Down mode 1 = WP# input can protect the Status Register or OTP Lock Down.
6	SEC	Sector / Block Protect		0	0 = BP2-BP0 protect 64-kB blocks 1 = BP2-BP0 protect 4-kB sectors
5	TB	Top / Bottom protect		0	0 = BP2-BP0 protect from the Top down 1 = BP2-BP0 protect from the Bottom up
4	BP2	Block Protect Bits		0	000b = No protection
3	BP1			0	
2	BP0			0	
1	WEL	Write Enable Latch	Volatile, Read only	0	0 = Not Write Enabled, no embedded operation can start 1 = Write Enabled, embedded operation can start
0	BUSY	Embedded Operation Status	Volatile, Read only	0	0 = Not Busy, no embedded operation in progress 1 = Busy, embedded operation in progress

Table 8.2 Status Register-2 (SR2)

Bits	Field	Function	Type	Default State	Description
7	SUS	Suspend Status	Volatile, Read Only	0	0 = Erase / Program not suspended 1 = Erase / Program suspended
6	CMP	Complement Protect	Non-volatile and Volatile versions	0	0 = Normal Protection Map 1 = Complementary Protection Map
5	LB3	Security Register Lock Bits	OTP	0	OTP Lock Bits 3:0 for Security Registers 3:0 0 = Security Register not protected 1 = Security Register protected
4	LB2			0	
3	LB1			0	
2	Reserve			0	
1	QE	Quad Enable	Non-volatile and Volatile versions	0	0 = Quad Mode Not Enabled, the WP# pin and HOLD# / RESET# are enabled 1 = Quad Mode Enabled, the IO2 and IO3 pins are enabled, and WP# and HOLD# / RESET# functions are disabled
0	Reserve			0	

8.2 N25Q008A

Table 8.3 Status Register-1 (SR1)

Bits	Field	Function	Type	Default State	Description
7	SRP0	Status Register Protect 0	Non-volatile and Volatile versions	0	0 = WP# input has no effect or Power Supply Lock Down mode 1 = WP# input can protect the Status Register or OTP Lock Down.
6	SEC	Sector / Block Protect		0	0 = BP2-BP0 protect 64-kB blocks 1 = BP2-BP0 protect 4-kB sectors
5	TB	Top / Bottom protect		0	0 = BP2-BP0 protect from the Top down 1 = BP2-BP0 protect from the Bottom up
4	BP2	Block Protect Bits		0	000b = No protection
3	BP1			0	
2	BP0			0	
1	WEL	Write Enable Latch	Volatile, Read only	0	0 = Not Write Enabled, no embedded operation can start 1 = Write Enabled, embedded operation can start
0	BUSY	Embedded Operation Status	Volatile, Read only	0	0 = Not Busy, no embedded operation in progress 1 = Busy, embedded operation in progress

Table 8.4 Status Register-2 (SR2)

Bits	Field	Function	Type	Default State	Description
7	SUS	Suspend Status	Volatile, Read Only	0	0 = Erase / Program not suspended 1 = Erase / Program suspended
6	CMP	Complement Protect	Non-volatile and Volatile versions	0	0 = Normal Protection Map 1 = Complementary Protection Map
5	LB3	Security Register Lock Bits	OTP	0	OTP Lock Bits 3:0 for Security Registers 3:0 0 = Security Register not protected 1 = Security Register protected
4	LB2			0	
3	LB1			0	
2	Reserve			0	
1	QE	Quad Enable	Non-volatile and Volatile versions	0	0 = Quad Mode Not Enabled, the WP# pin and HOLD# / RESET# are enabled 1 = Quad Mode Enabled, the IO2 and IO3 pins are enabled, and WP# and HOLD# / RESET# functions are disabled
0	Reserve				

8.3 N25Q016B

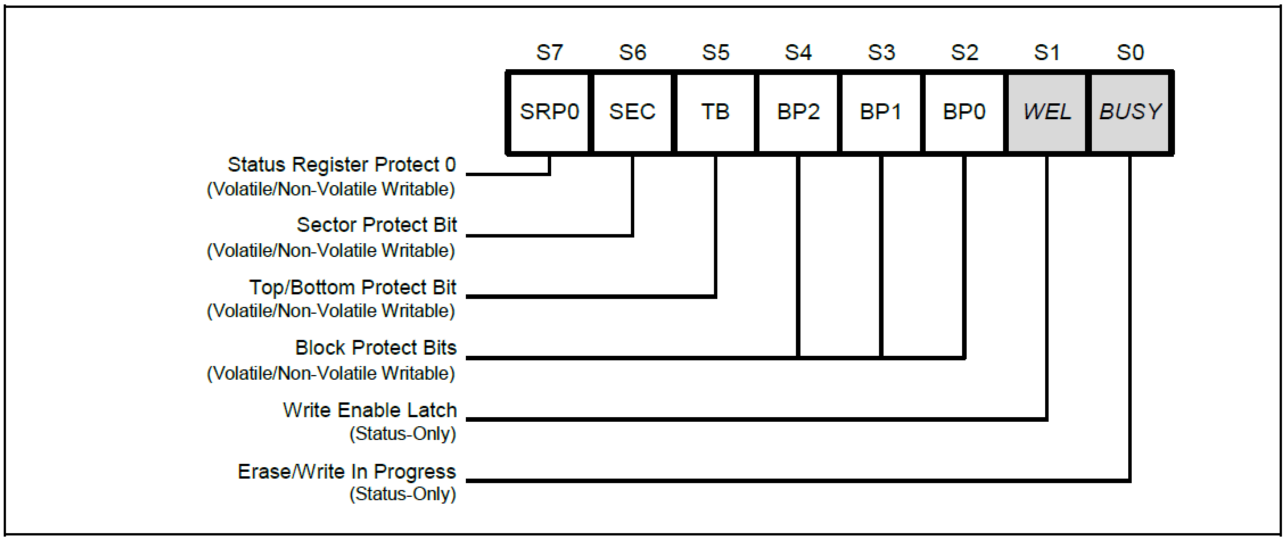


Figure 8.1 Status Register-1 (SR1)

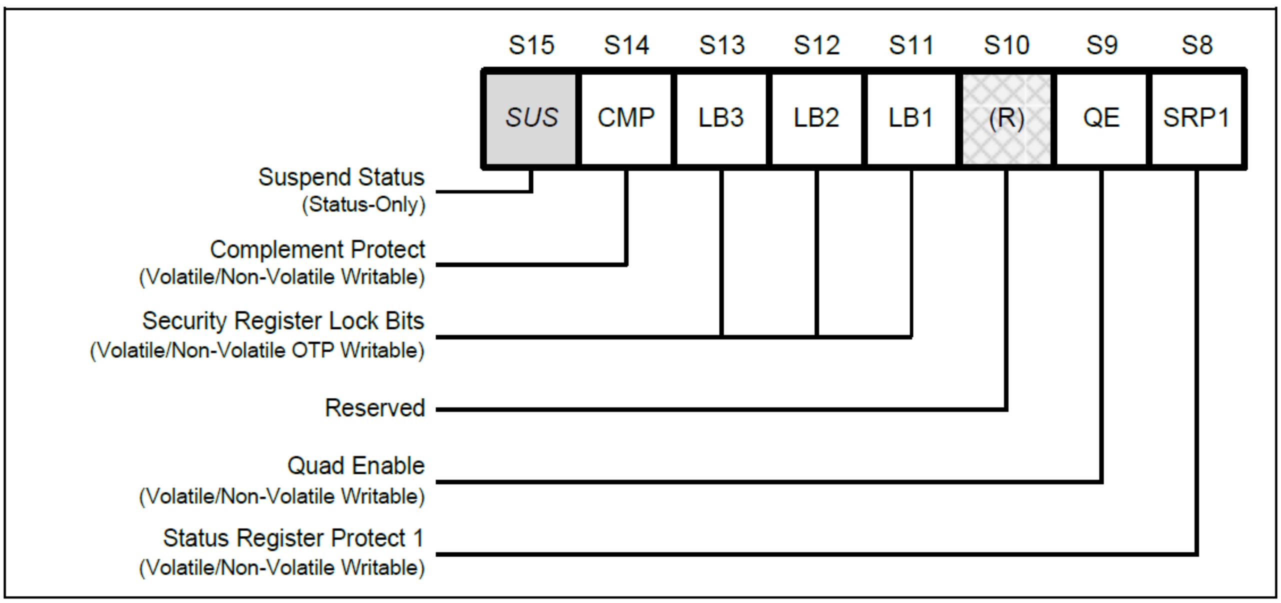


Figure 8.2 Status Register-2 (SR2)

8.4 N25Q032C

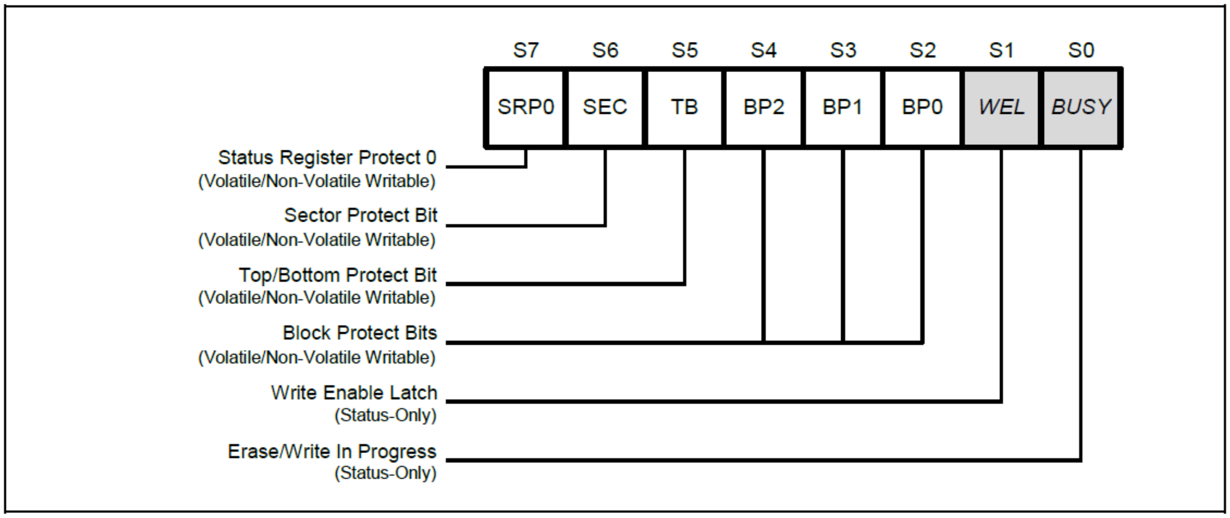


Figure 8.3 Status Register-1 (SR1)

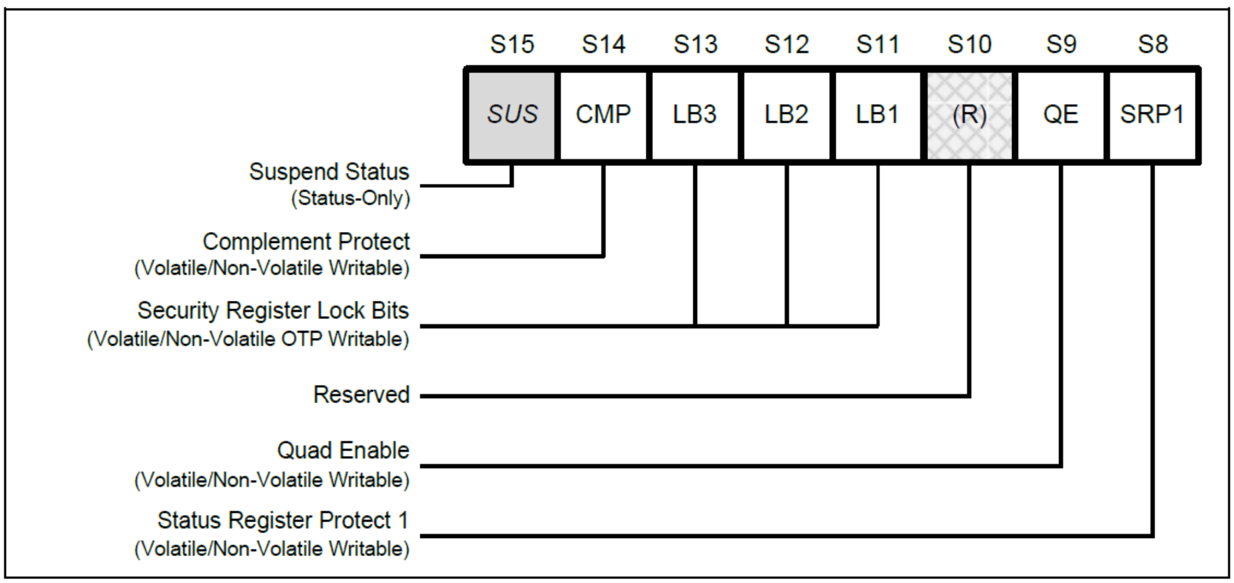


Figure 8.4 Status Register-2 (SR2)

9. FUNCTIONAL DESCRIPTION

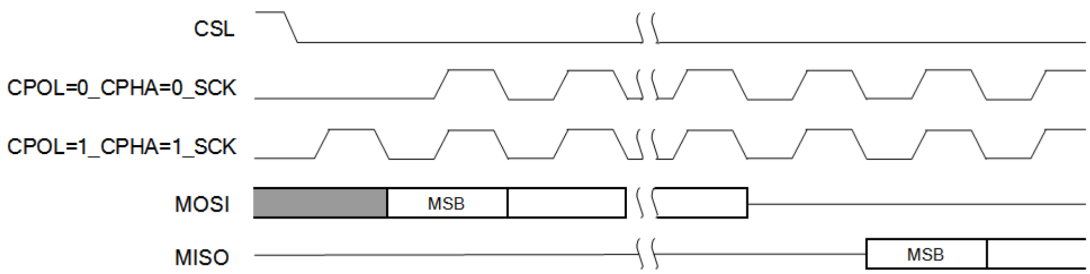
9.1 SPI Modes

N25Q series can be driven by an SPI bus master in either of the two following clock modes.

- **Mode 0** with Clock Polarity (CPOL) = 0 and, Clock Phase (CPHA) = 0
- **Mode 3** with CPOL = 1 and, CPHA = 1

For these two modes, input data is always latched in on the rising edge of SCK and the output data is always available on the falling edge of SCK. The difference between the two modes is the clock polarity when the bus master is in standby mode and not transferring any data.

- SCK will stay at logic low state with CPOL = 0, CPHA = 0
- SCK will stay at logic high state with CPOL = 1, CPHA = 1



Timing diagrams throughout the rest of the document are generally shown as both mode 0 and 3 by showing SCK as both high and low at the fall of CSL. In some cases a timing diagram may show only mode 0 with SCK low at the fall of CSL. In such case, mode 3 timing simply means clock is high at the fall of CSL so no SCK rising edge set up or hold time to the falling edge of CSL is needed for mode 3. SCK cycles are measured (counted) from one falling edge of SCK to the next falling edge of SCK. In mode 0 the beginning of the first SCK cycle in a command is measured from the falling edge of CSL to the first falling edge of SCK because SCK is already low at the beginning of a command.

9.2 Dual SPI Modes

N25Q series supports Dual SPI Operation when using Fast Dual I/O (BBh) instruction. This feature allows data to be transferred from the device at twice the rate possible with the standard SPI. This instruction is ideal for quickly downloading code to RAM upon Power-up (code-shadowing) or for executing non-speed-critical code directly from the SPI bus (XIP). When using Dual SPI command, the MOSI and MISO pins become bidirectional IO0 and IO1 respectively.

9.3 Quad SPI Modes

N25Q series supports Quad SPI operation when using Fast Read Quad I/O (EBh) instruction. This instruction allows data to be transferred to or from the device four times the rate of ordinary Serial Flash. The Quad Read instruction offer a significant improvement in continuous and random access transfer rates allowing fast code-shadowing to RAM or execution directly from the SPI bus (XIP). When using Quad SPI instruction, the MOSI and MISO pins become bidirectional IO0 and IO1, and the WPL and HLD pins become IO2 and IO3 respectively.

10. ELECTRICAL CHARACTERISTICS

10.1 Absolute Maximum Rating

Symbol	Parameter	Rated Value	Unit
V_{DD} - V_{SS}	Supply voltage	-0.6 ~ +4.0	V
V_{IN}	Input voltage	V_{SS} -0.6V ~ V_{DD} +0.3	V
Top	Operating Temperature	0 ~ +70	°C
Tst	Storage Temperature	-25 ~ +85	°C

10.2 DC Characteristics

(All refer VDD =3.0V, ambient temperature T_A=25°C unless otherwise specified.)

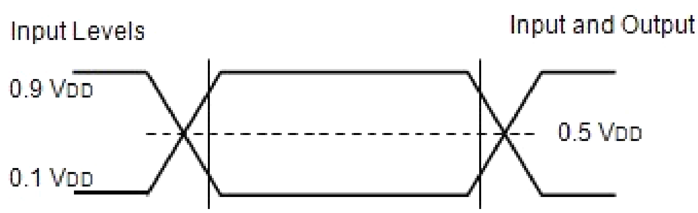
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{DD}	Operating voltage	2.7	3.3	3.6	V	F_R=104MHz,f_R=50MHz
C_{IN}	Input Capacitance	-	-	6	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	-	-	8	pF	VOUT = 0V
I_{LI}	Input Leakage	-	-	±2	uA	
I_{LO}	I/O Leakage	-	-	±2	uA	
I_{CC1}	Standby Current	-	15	25	uA	CSL = V_{DD}, V_{IN}= V_{SS} or V_{DD}
I_{CC2}	Power-down Current	-	2	5	uA	CSL = V_{DD}, V_{IN} = V_{SS} or V_{DD}
I_{CC3}	Current Read Data / Dual/Quad Read 50MHz	-	-	15	mA	C = 0.1 V_{DD} / 0.9 V_{DD} MISO = Open
I_{CC3}	Current Read Data / Dual/Quad Read 80MHz	-	-	18	mA	C = 0.1 V_{DD} / 0.9 V_{DD} MISO = Open
I_{CC3}	Current Read Data / Dual/Quad Read 104MHz	-	-	20	mA	C = 0.1 V_{DD} / 0.9 V_{DD} MISO = Open
I_{CC4}	Current Page Program	-	8	12	mA	CSL = V_{DD}
I_{CC5}	Current Write Status Register	-	20	25	mA	CSL = V_{DD}
I_{CC6}	Current Sector/Block Erase	-	20	25	mA	CSL = V_{DD}
I_{CC7}	Current Chip Erase	-	20	25	mA	CSL = V_{DD}
I_{CC8}	Current High Performance	-	500	800	uA	
V_{IL}	Input Low Voltage	-0.5		V_{DD} x0.3	V	
V_{IH}	Input High Voltage	V_{DD} x0.7	-	-	V	
V_{OL}	Output Low Voltage	-	-	0.2	V	I_{OL} = 100 uA
V_{OH}	Output High Voltage	V_{DD}-0.2	-	-	V	I_{OH} = -100 uA

10.3 Voltage vs. Frequency

Symbol	Parameter	Min.	Unit
V_{OP32M}	Minimum Operating Voltage at SCK=32MHz	2.35	V
V_{OP16M}	Minimum Operating Voltage at SCK=16MHz	2.15	V
V_{OP1M}	Minimum Operating Voltage at SCK=1MHz	1.95	V

10.4 AC Measurement Conditions

Symbol	Parameter	Min.	Max.	Unit
C_L	Load Capacitance	-	30	pF
T_R, T_F	Input Rise and Fall Times	-	5	ns
V_{IN}	Input Pulse Voltages	0.1 V_{DD} to 0.9 V_{DD}		V
I_N	Input Timing Reference Voltages	0.3 V_{DD} to 0.7 V_{DD}		V
O_{UT}	Output Timing Reference Voltages	0.5 V_{DD} to 0.5 V_{DD}		V

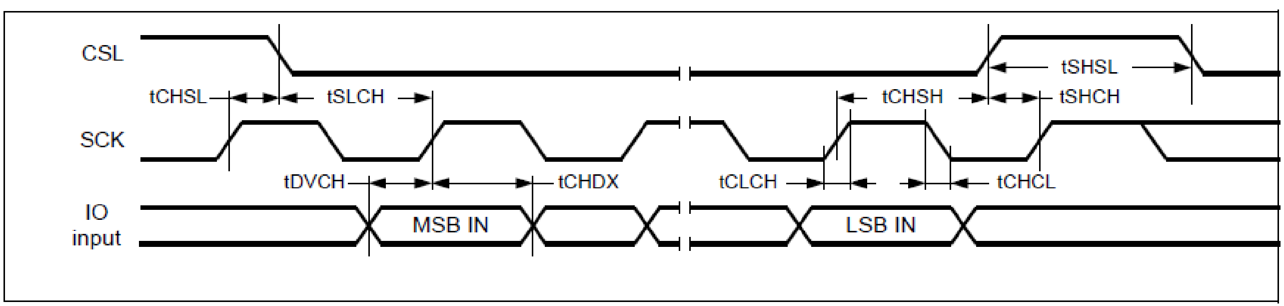


10.5 AC Characteristics

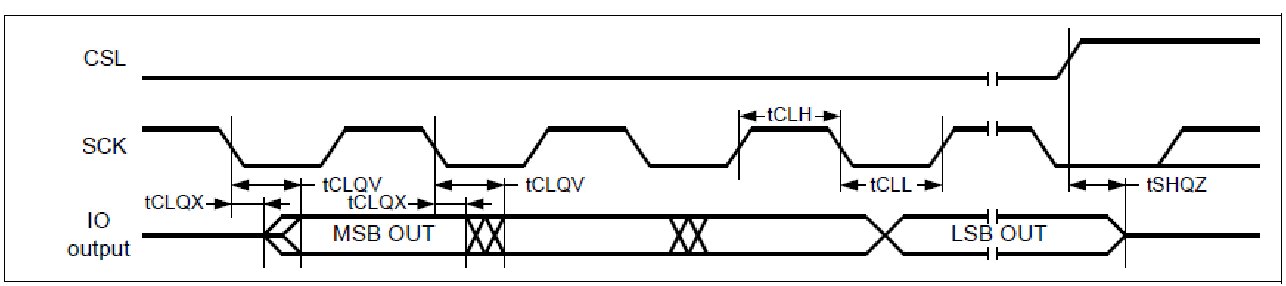
Symbol	Parameter	Min.	Typ.	Max.	Unit
F_R	Clock frequency for all other instructions except Read data instructions (03h)	D.C.	-	104	MHz
f_R	Clock frequency for Read Data instruction (03h)	D.C.	-	50	MHz
tCLH, tCLL	Clock High, Low Time for all instructions except for Read Data (03h)	4	-	-	ns
tCRLH, tCRLL	Clock High, Low Time for Read Data (03h) instruction	6	-	-	ns
tCLCH	Clock Rise Time peak to peak	0.1	-	-	V/ns
tCHCL	Clock Fall Time peak to peak	0.1	-	-	V/ns
tSLCH	CSL Active Setup Time relative to SCK	5	-	-	ns
tCHSL	CSL Not Active Hold Time relative to SCK	5	-	-	ns
tDVCH	Data In Setup Time	2	-	-	ns
tCHDX	Data In Hold Time	5	-	-	ns
tCHSH	CSL Active Hold Time relative to SCK	5	-	-	ns
tSHCH	CSL Not Active Setup Time relative to SCK	5	-	-	ns

Symbol	Parameter	Min.	Typ.	Max.	Unit
tSHSL1	CSL Deselect Time (for Read)	10	-	-	ns
tSHSL2	CSL Deselect Time (for Erase or Program or write)	50	-	-	ns
tSHQZ	Output Disable Time	-	-	7	ns
tCLQV	Clock Low to Output Valid	-	-	7	ns
tCLQX	Output Hold Time	2	-	-	ns
tDP	CSL High to Power-down Mode	-	-	3	µs
tRES1	CSL High to Standby Mode without ID Read	-	-	8	µs
tRES2	CSL High to Standby Mode with ID Read	-		6	µs
tSUS	CSL High to next Instruction after Suspend	-	-	20	µs
tSUS	CSL High to next Instruction after Reset	-	-	30	µs
tW	Write Status Register Time	-	10	100	ms
tPUW	Power ON delay before 1st Write Instruction	1	-	10	ms
tPP	Page Program Time	-	0.5	3	ms
tSE	Sector Erase Time (4KB)	-	50	300	ms
tBE2	Block Erase Time (64KB)	-	300	2,000	ms
tCE	Chip Erase Time	Depends on Memory Size			

10.6 Serial Input Timing

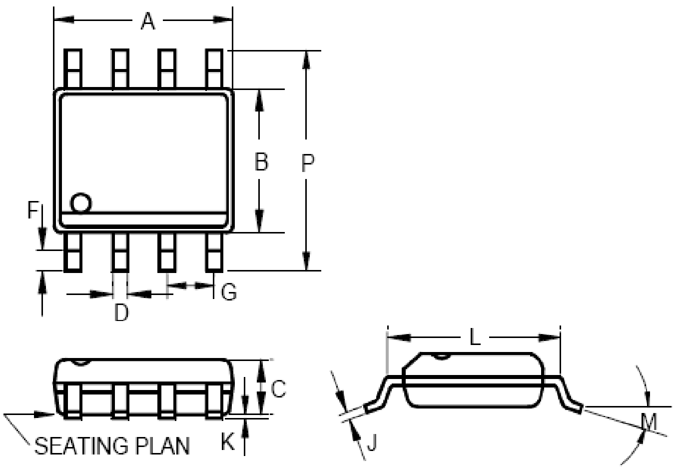


10.7 Serial Output Timing



11. PACKAGE DIMENSION

11.1 8-Pin Plastic SOP (150 mil)



	INCHES			MILLIMETERS		
	MIN	TYP	MAX	MIN	TYP	MAX
A	0.183	-	0.202	4.65	-	5.13
B	0.144	0.150	0.163	3.66	3.81	4.14
C	0.068	-	0.074	1.35	-	1.88
D	0.010	-	0.020	0.25	-	0.51
F	0.015	-	0.035	0.38	-	0.89
G	0.050 BSC			1.27 BSC		
J	0.007	-	0.010	0.19	-	0.25
K	0.005	-	0.010	0.13	-	0.25
L	0.189	-	0.205	4.80	-	5.21
M	-	-	8°	-	-	8°
P	0.228	-	0.244	5.79	-	6.20

Note: For 8-pin SOP IC, 100 units per tube.

12. ORDERING INFORMATION

P/N	Package Type	Package Width	Shipping	Remarks
N25Q004AS8	SOP8	150 mil	Tape & Reel: 2.5K pcs per Reel Tube: 100 pcs per Tube	Blank
N25Q004AS8-xxxx *1	SOP8	150 mil		Programmed
N25Q008AS8	SOP8	150 mil		Blank
N25Q008AS8-xxxx *1	SOP8	150 mil		Programmed
N25Q016BS8	SOP8	150 mil		Blank
N25Q016BS8-xxxx *1	SOP8	150 mil		Programmed
N25Q032CS8	SOP8	150 mil		Blank
N25Q032CS8-xxxx *1	SOP8	150 mil		Programmed

**1 "xxxx": Code number*