## NY8A053E

## 12 I／O 8－bit EPROM－Based MCU

## Version 1.2

Nov．30， 2022

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## Revision History

| Version | Date | Description | Modified Page |
| :---: | :--- | :--- | :---: |
| 1.0 | $2020 / 11 / 27$ | Preliminary edition. | - |
| 1.1 | $2021 / 09 / 30$ | 1. Revised PWM channels <br> 2. RBIAS_L and RBIAS_H must set as "00" before sleep or halt mode <br> 3. Revised IHALT @ VDD=3V, Halt mode, WDT enabled | 11 <br> 26,53 <br> 82 |
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## 1．概述

NY8A053E是以EPROM作為記憶體的 8 位元微控制器，專為多IO產品的應用而設計，例如遙控器，風扇／燈光控制或是遊樂器周邊等等。採用CMOS製程並同時提供客戶低成本，高性能等顯著優勢。NY8A053E核心建立在RISC精簡指令集架構可以很容易地做編輯和控制，共有 55 條指令。除了少數指令需要 2 個時序，大多數指令都是 1 個時序即能完成，可以讓使用者輕鬆地以程式控制完成不同的應用。因此非常適合各種中低記憶容量但又複雜的應用。

在I／O的資源方面，NY8A053E有 12 根彈性的雙向I／O腳，每個I／O腳都有單獨的暫存器控制為輸入或輸出腳。而且每一個 $/$ O腳位都有附加的程式控制功能如上拉或下拉電阻或開漏極（Open－Drain）輸出。此外針對紅外線搖控的產品方面，NY8A053E內建了可選擇頻率的紅外載波發射口。

NY8A053E有兩組計時器，可用系統頻率當作一般的計時的應用或者從外部訊號觸發來計數。另外NY8A053E提供 4組 10 位元解析度的PWM輸出或者蜂鳴器輸出，可用來驅動馬達，LED，或蜂鳴器等等。

NY8A053E採用雙時鐘機制，高速振盪或者低速振盪都可以分別選擇內部RC振盪或外部Crystal輸入。在雙時鐘機制下，NY8A053E可選擇多種工作模式如正常模式（Normal），慢速模式（Slow mode），待機模式（Standby mode）與睡眠模式（Halt mode）可節省電力消耗延長電池壽命。並且微控制器在使用內部RC高速振盪時，低速振盪可以同時使用外部精準的Crystal計時。可以維持高速處理同時又能精準計算真實時間。

在省電的模式下如待機模式（Standby mode）與睡眠模式（Halt mode）中，有多種事件可以觸發中斷喚醒NY8A053E進入正常操作模式（Normal）或 慢速模式（Slow mode）來處理突發事件。

## 1.1 功能

－寬廣的工作電壓：
$>2.0 \mathrm{~V} \sim 5.5 \mathrm{~V}$＠系統頻率 $\leqq 8 \mathrm{MHz}$ 。
＞ $2.2 \mathrm{~V} \sim 5.5 \mathrm{~V}$＠系統頻率 $>8 \mathrm{MHz}$ 。

- 萈廣的工作温度：$-40^{\circ} \mathrm{C} \sim 85^{\circ} \mathrm{C}$ 。
- 1 Kx 14 bits EPROM 。
- 64 bytes SRAM 。
- 内建準確的低電壓偵測電路（LVD）。14 階（2．2V～4．15V）
- 內建準確的電壓比較器（Voltage Comparator）。
- 12 根可分別單獨控制輸入輸出方向的 $/$／O腳（GPIO），PA［3：0］，PB［7：0］。
- $\mathrm{PA}[3: 0]$ 及 $\mathrm{PB}[3: 0]$ 可選擇輸入時使用內建下拉電阻。
- PB［7：0］可選擇上拉電阻或開漏極輸出（Open－Drain）。
- PB［3］可選擇當作輸入或開漏極輸出（Open－Drain）。
- 8 層程式堆棧（Stack）。
- 存取資料有直接或間接定址模式。
- 一組 8 位元上數計時器（TimerO）包含可程式化的頻率預除線路。
- 一組 10 位元下數計時器（Timer1）可選重複載入或連續下數計時。
- 4 個 10 位元的脈衝寬度調變輸出（PWM1～PWM4），PWM1／2／3／4 共用Timer1。
- 一個蜂鳴器輸出（BZ1）。
- 38／57KHz紅外線載波頻率可供選擇，同時載波之極性也可以根據數據作選擇。
- 紅外線載波發射 $\square$ 。
- 內建上電復位電路（POR）。
- 內建低壓復位功能（LVR）。
- 內建看門狗計時（WDT），可由程式韎體控制開關。
- 雙時鐘機制，系統可以隨時切換高速振盪或者低速振盪。
＞高速振盪：E＿HXT（超過 6 MHz 外部高速石英振盪）
E＿XT（455K～6MHz外部石英振盪）
I＿HRC（1～20MHz內部高速RC振盪）
＞低速振盪：E＿LXT（32KHz外部低速石英振盪）
I＿LRC（內部 32KHz低速RC振盪）
－四種工作模式可随系統需求調整電流消耗：正常模式（Normal），慢速模式（Slow mode），待機模式（Standby mode）與 睡眠模式（Halt mode）。
－六種硬體中斷：
$>$ Timer0 溢位中斷。
＞Timer1 借位中斷。
$>$ WDT 中斷。
$>\mathrm{PB}$ 輸入狀態改變中斷。
$>$ 外部中斷輸入。
$>$ 低電壓偵測中斷。
－NY8A053E在待機模式（Standby mode）下的六種喚醒中斷：
＞Timer0 溢位中斷。
＞Timer1 借位中斷。
＞WDT 中斷。
＞PB 輸入狀態改變中斷。
＞外部中斷輸入。
＞低電壓偵測中斷。
－NY8A053E在睡眠模式（Halt mode）下的三種喚醒中斷：
＞WDT 中斷。
＞ PB 輸入狀態改變中斷。
＞外部中斷輸入。


## 1．2 NY8A053E 與 NY8A053D 的主要差異

| Item | Function | NY8A053E | NY8A053D |
| :---: | :--- | :---: | :---: |
| 1 | PortB input pull－high resistor | PB［7：0］ | PB［7：4］，PB［2：0］ |
| 2 | Comparator | Yes | --- |
| 3 | Low Voltage Detector（LVD）voltage level | 14 voltage levels | --- |
| 4 | Comparator structure | shared with LVD | --- |
| 5 | PortB wake－up default status | default：disable | default：enable |
| 6 | Input Schmitt Trigger | Enable／Disable | －－－ |
| 7 | PWM | $10-b i t ~ P W M ~ x 4 ~$ | 8－bit PWM x1 |

## 1. General Description

NY8A053E is an EPROM based 8-bit MCU tailored for I/O based applications like remote controllers, fan/light controller, game controllers, toy and various controllers.NY8A053E adopts advanced CMOS technology to provide customers remarkable solution with low cost and high performance. RISC architecture is applied to NY8A053E and it provides 55 instructions. All instructions are executed in single instruction cycle except program branch and skip instructions which will take two instruction cycles. Therefore, NY8A053E is very suitable for those applications that are sophisticated but compact program size is required.

As NY8A053E address I/O type applications, it can provide 12 I/O pins for applications which require abundant input and output functionality. Moreover, each I/O pin may have additional features, like Pull-High/Pull-Low resistor and open-drain output type through programming. Moreover, NY8A053E has built-in infrared (IR) carrier generator with selectable IR carrier frequency and polarity for applications which demand remote control feature.

NY8A053E also provides 2 sets of timers which can be used as regular timer based on system oscillation or event counter with external trigger clock. Moreover, NY8A053E provides 4 set of 10-bit resolution Pulse Width Modulation (PWM) output and buzzer output in order to drive motor/LED and buzzer.

NY8A053E employs dual-clock oscillation mechanism, either high oscillation or low oscillation can be derived from internal resistor/capacitor oscillator or external crystal oscillator. Moreover, based on dual-clock mechanism, NY8A053E provides kinds of operation mode like Normal mode, Slow mode, Standby mode and Halt mode in order to save power consumption and lengthen battery operation life. Moreover, it is possible to use internal high-frequency oscillator as CPU operating clock source and external 32 KHz crystal oscillator as timer clock input, so as to accurate count real time and maintain CPU working power.

While NY8A053E operates in Standby mode and Halt mode, kinds of event will issue interrupt requests and can wake-up NY8A053E to enter Normal mode and Slow mode in order to process urgent events.

### 1.1 Features

- Wide operating voltage range:
$>2.0 \mathrm{~V} \sim 5.5 \mathrm{~V}$ @system clock $\leqq 8 \mathrm{MHz}$.
> $2.2 \mathrm{~V} \sim 5.5 \mathrm{~V}$ @system clock $>8 \mathrm{MHz}$.
- Wide operating temperature: $-40^{\circ} \mathrm{C} \sim 85^{\circ} \mathrm{C}$.
- $1 \mathrm{~K} \times 14$ bits EPROM.
- 64 bytes SRAM.
- 12 general purpose I/O pins (GPIO), PA[3:0], PB[7:0], with independent direction control.
- $\quad \mathrm{PA}[3: 0]$ and $\mathrm{PB}[3: 0]$ have features of Pull-Low resistor for input pin.
- $\mathrm{PB}[7: 0]$ have features of Pull-High resistor, and open-drain output.
- $\mathrm{PB}[3]$ have feature of input or open-drain output.
- 8-level hardware Stack.
- Direct and indirect addressing modes for data access.
- One 8-bit up-count timer (Timer0) with programmable prescaler.
- One 10-bit reload or continuous down-count timers (Timer1).
- Four 10-bit resolution PWM (PWM1~4) outputs.
- One buzzer (BZ1) output.
- Selectable $38 / 57 \mathrm{KHz}$ IR carrier frequency and high/low polarity according to data value.
- Built-in high-precision Low-Voltage Detector (LVD).
- Built-in high-precision Voltage Comparator.
- Built-in Power-On Reset (POR).
- Built-in Low-Voltage Reset (LVR).
- Built-in Watch-Dog Timer (WDT) enabled/disabled by firmware control.
- Dual-clock oscillation: System clock can switch between high oscillation and low oscillation.
> High oscillation: E_HXT (External High Crystal Oscillator, above 6MHz)
E_XT (External Crystal Oscillator, 455K~6MHz)
I_HRC (Internal High Resistor/Capacitor Oscillator ranging from 1M~20MHz)
> Low oscillation: E_LXT (External Low Crystal Oscillator, about 32KHz)
I LRC (Internal 32KHz oscillator)
- Four kinds of operation mode to reduce system power consumption:
> Normal mode, Slow mode, Standby mode and Halt mode.
- Six hardware interrupt events:
> Timer0 overflow interrupt.
> Timer1 underflow interrupt.
$>$ WDT timeout interrupt.
$>$ PB input change interrupt.
$>$ External interrupt.
> LVD interrupt
- Six interrupt events to wake-up NY8A053E from Standby mode:
$>$ TimerO overflow interrupt.
$>$ Timer1 underflow interrupt.
$>$ WDT timeout interrupt
$>$ PB input change interrupt.
$>$ External interrupt.
$>$ LVD interrupt
- Three interrupt events to wake-up NY8A053E from Halt mode:
> WDT timeout interrupt.
> PB input change interrupt.
> External interrupt.


### 1.2 Block Diagram



### 1.3 Pin Assignment

NY8A053E provides three kinds of package type which are SOP14, DIP14 and SOP8.


Figure 1 Package pin assignment

### 1.4 Pin Description

| Pin Name | I/O | Description |
| :---: | :---: | :---: |
| PA0/ PWM2 | I/O | PAO is a bidirectional I/O pin. <br> PAO is output of PWM2 signal by configuration words. |
| PA1/ PWM2 | I/O | PA1 is a bidirectional I/O pin. <br> PA1 is output of PWM2 signal by configuration words. |
| PA2/ PWM4 | I/O | PA2 is a bidirectional I/O pin. <br> PA2 is output of PWM4 signal by configuration words. |
| PA3/ PWM3 | I/O | PA3 is a bidirectional I/O pin. <br> PA3 is output of PWM3 signal by configuration words. |
| PB0/ PWM4 / INT/ SDI | I/O | PBO is a bidirectional I/O pin. <br> PBO is output of PWM4 signal by configuration words. <br> PBO is input pin of external interrupt when EIS=1 \& INTIE=1. <br> PBO can be programming pad SDI. |
| PB1/ PWM3/ IR/ CMPO/ SDO | I/O | PB1 is a bidirectional I/O pin. <br> PB1 can be the output of PWM3, IR or comparator. <br> PB1 can be programming pad SDO. |
| PB2/ EX_CKI/ PWM1/ BZ1/ SCK | I/O | PB2 is a bidirectional I/O pin. <br> It also can be timer clock source EX_CKI. <br> PB2 can be programming pad SCK. <br> PB2 is output of PWM1 signal by configuration words. <br> PB2 is output of Buzzer signal by configuration words. <br> PWM has higher priority over Buzzer functions. |
| PB3/ RSTb/ VPP | I/O | PB3 is an input pin or open-drain output pin. <br> It can be reset pin RSTb. If RSTb pin is low, it will reset NY8A053E. <br> If this pin is more than 7.75 V , it also can make NY8A053E enter EPROM programming mode. |
| PB4/ Xout | I/O | PB4 is a bidirectional I/O pin if I_HRC and I_LRC are adopted. PB4 also can be output of instruction clock. <br> PB4 is output of external crystal if $E_{-}$HXT, E_XT or E_LXT is adopted. |
| PB5/ Xin | I/O | PB5 is a bidirectional I/O pin if I_HRC and I_LRC are adopted. PB5 is input of external crystal if E_HXT, E_XT or E_LXT is adopted. |
| PB6/ PWM1 | I/O | PB6 is a bidirectional I/O pin. <br> PB6 is output of PWM signal by configuration words. |
| PB7/ BZ1 | I/O | PB7 is a bidirectional I/O pin. <br> PB7 is output of Buzzer signal by configuration words. |
| VDD | - | Positive power supply. |
| VSS | - | Ground. |

## 2. Memory Organization

NY8A053E memory is divided into two categories: one is program memory and the other is data memory.

### 2.1 Program Memory

The program memory space of NY8A053E is 1K words. Therefore, the Program Counter (PC) is 10-bit wide in order to address any location of program memory.

Some locations of program memory are reserved as interrupt entrance. Power-On Reset vector is located at $0 \times 000$. Software interrupt vector is located at $0 \times 001$. Internal and external hardware interrupt vector is located at $0 \times 008$.

NY8A053E provides instruction CALL, GOTOA, CALLA to address 256 location of program space. NY8A053E provides instruction GOTO to address 512 location of program space. NY8A053E also provides instructions LCALL and LGOTO to address any location of program space.

When a call or interrupt is happening, next ROM address is written to top of the stack, when RET, RETIA or RETIE instruction is executed, the top of stack data is read and load to PC.

NY8A053E program ROM address $0 \times 3$ FE $\sim 0 \times 3$ FF are reserved space, if user tries to write code in these addresses will get unexpected false functions.

NY8A053E program ROM address $0 \times 00 \mathrm{E} \sim 0 \times 00 \mathrm{~F}$ are preset rolling code can be released and used as normal program space.


Figure 2 Program Memory Address Mapping

### 2.2 Data Memory

According to instructions used to access data memory, the data memory can be divided into three kinds of categories: one is R-page Special-function Register (SFR) + General Purpose Register (GPR), another is F-page SFR and the other is S-page SFR. GPR are made of SRAM and user can use them to store variables or intermediate results.

R-page data memory is divided into 4 banks and can be accessed directly or indirectly through a SFR register which is File Select Register (FSR). FSR[7:6] are used as Bank register BK[1:0] to select one bank out of the 4 banks.

R-page register can be divided into addressing mode: direct addressing mode and indirect addressing mode.
The indirect addressing mode of data memory access is described in the following graph. This indirect addressing mode is implied by accessing register INDF. The bank selection is determined by FSR[7:6] and the location selection is from FSR[5:0].


Figure 3 Indirect Addressing Mode of Data Memory Access

The direct addressing mode of data memory access is described below. The bank selection is determined by FSR[7:6] and the location selection is from instruction op-code[5:0] immediately.


Figure 4 Direct Addressing Mode of Data Memory Access

R-page SFR can be accessed by general instructions like arithmetic instructions and data movement instructions. The R-page SFR occupies address from $0 x 0$ to $0 x F$ of Bank 0 . However, the same address range of Bank 1, Bank 2 and Bank 3 are mapped back to Bank 0. In other words, R-page SFR physically existed at Bank 0. The GPR physically occupy address from $0 \times 10$ to $0 \times 3 F$ of Bank 0 and $0 \times 10$ to $0 \times 1 \mathrm{~F}$ of Bank 1. Other banks in address from $0 \times 10$ to $0 \times 3 F$ are mapped back as the Table 1 shows.

The NY8A053E register name and address mapping of R-page SFR are described in the following table.

| FSR[7:6] <br> Address | $\begin{gathered} 00 \\ \text { (Bank 0) } \end{gathered}$ | $01$ (Bank 1) | $\begin{gathered} 10 \\ \text { (Bank 2) } \end{gathered}$ | 11 (Bank 3) |
| :---: | :---: | :---: | :---: | :---: |
| $0 \times 0$ | INDF | The same mapping as Bank 0 |  |  |
| 0x1 | TMR0 |  |  |  |
| 0x2 | PCL |  |  |  |
| 0x3 | STATUS |  |  |  |
| 0x4 | FSR |  |  |  |
| 0x5 | PORTA |  |  |  |
| 0x6 | PORTB |  |  |  |
| 0x7 | - |  |  |  |
| 0x8 | PCON |  |  |  |
| 0x9 | BWUCON |  |  |  |
| 0xA | PCHBUF |  |  |  |
| 0xB | ABPLCON |  |  |  |
| 0xC | BPHCON |  |  |  |
| 0xD | - |  |  |  |
| 0xE | INTE |  |  |  |
| 0xF | INTF |  |  |  |
| 0x10~0x1F | General Purpose Register | General Purpose Register | Mapped to bankO | Mapped to bank1 |
| $0 \times 20 \sim 0 \times 3 F$ | General Purpose Register |  | Mapped to bank0 |  |

Table 1 R-page SFR Address Mapping

F-page SFR can be accessed only by instructions IOST and IOSTR. S-page SFR can be accessed only by instructions SFUN and SFUNR. FSR[7:6] bank select bits are ignored while F-page and S-page register is accessed. The register name and address mapping of F-page and S-page are depicted in the following table.

| SFR Category <br> Address | F-page SFR | S-page SFR |
| :---: | :---: | :---: |
| $0 \times 0$ | - | TMR1 |
| 0x1 | - | T1CR1 |
| 0x2 | - | T1CR2 |
| 0x3 | - | PWM1DUTY |
| 0x4 | - | PS1CV |
| $0 \times 5$ | IOSTA | BZ1CR |
| 0x6 | IOSTB | IRCR |
| 0x7 | - | TBHP |
| 0x8 | - | TBHD |
| 0x9 | - | - |
| 0xA | PS0CV | P2CR1 |
| 0xB | - | - |
| 0xC | BODCON | PWM2DUTY |
| 0xD | - | TMRH |
| 0xE | CMPCR | TM34RH |
| 0xF | PCON1 | OSCCR |
| 0x10 |  |  |
| $0 \times 11$ |  | P3CR1 |
| 0x12 |  |  |
| $0 \times 13$ |  | PWM3DUTY |
| 0x14 |  |  |
| $0 \times 15$ |  |  |
| $0 \times 16$ |  | P4CR1 |
| $0 \times 17$ |  |  |
| $0 \times 18$ |  | PWM4DUTY |

Table 2 F-page and S-page SFR Address Mapping

## 3. Function Description

This chapter will describe the detailed operations of NY8A053E.

### 3.1 R-page Special Function Register

### 3.1.1 INDF (Indirect Addressing Register)

| Name | SFR Type | Addr. | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| INDF | R | 0x0 | INDF[7:0] |  |  |  |  |  |  |  |
| R/W Property |  |  | R/W |  |  |  |  |  |  |  |
| Initial Value |  |  | xxxxxxxx |  |  |  |  |  |  |  |

The register INDF is not physically existed and it is used as indirect addressing mode. Any instruction accessing INDF actually accesses the register pointed by register FSR

### 3.1.2 TMR0 (Timer0 Register)

| Name | SFR Type | Addr. | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| TMR0 | R | 0x1 | TMR0[7:0] |  |  |  |  |  |  |  |
| R/W Property |  |  | R/W |  |  |  |  |  |  |  |
| Initial Value |  |  | XXXXXXXX |  |  |  |  |  |  |  |

When read the register TMRO, it actually read the current running value of Timer0.
Write the register TMR0 will change the current value of Timer0.
Timer0 clock source can be from instruction clock Finst, or from external pin EX_CKI, or from Low Oscillator Frequency according to TOMD and configuration word setting.

### 3.1.3 PCL (Low Byte of PC[9:0])

| Name | SFR Type | Addr. | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| PCL | R | $0 \times 2$ | PCL[7:0] |  |  |  |  |  |  |  |
| R/W Property |  |  | R/W |  |  |  |  |  |  |  |
| Initial Value |  |  |  |  |  |  |  |  |  |  |

The register PCL is the least significant byte (LSB) of 10 -bit PC. PCL will be increased by one after one instruction is executed except some instructions which will change PC directly. The high byte of PC, i.e. $\mathrm{PC}[9: 8]$, is not directly accessible. Update of $\mathrm{PC}[9: 8]$ must be done through register PCHBUF.

For GOTO instruction, PC[8:0] is from instruction word and PC[9] is loaded from PCHBUF[1]. For CALL instruction, $\mathrm{PC}[7: 0]$ is from instruction word and $\mathrm{PC}[9: 8]$ is loaded from PCHBUF[1:0]. Moreover the next PC address, i.e. PC+1, will push onto top of Stack. For LGOTO instruction, PC[9:0] is from instruction word.

For LCALL instruction, PC[9:0] is from instruction word. Moreover the next PC address, i.e. PC+1, will push onto top of Stack.

NY8A053E

### 3.1.4 STATUS (Status Register)

| Name | SFR Type | Addr. | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| STATUS | R | 0x3 | GP7 | GP6 | GP5 | /TO | /PD | Z | DC | C |
| R/W Property |  |  | R/W | R/W | R/W | R/W(*2) | R/W(*1) | R/W | R/W | R/W |
| Initial Value |  |  | 0 | 0 | 0 | 1 | 1 | X | X | X |

The register STATUS contains result of arithmetic instructions and reasons to cause reset.
C: Carry/Borrow bit
$\mathrm{C}=1$, carry is occurred for addition instruction or borrow is not occurred for subtraction instruction.
$\mathrm{C}=0$, carry is not occurred for addition instruction or borrow is occurred for subtraction instruction.
DC: Half Carry/half Borrow bit
DC=1, carry from the 4th LSB is occurred for addition instruction or borrow from the 4th LSB is not occurred for subtraction instruction.
$\mathrm{DC}=0$, carry from the 4th LSB is not occurred for addition instruction or borrow from the 4th LSB is occurred for subtraction instruction.

Z: Zero bit
$Z=1$, result of logical operation is zero.
$Z=0$, result of logical operation is not zero.
/PD: Power down flag bit
/PD=1, after power-up or after instruction CLRWDT is executed.
$/ P D=0$, after instruction SLEEP is executed.
/TO: Time overflow flag bit
/TO=1, after power-up or after instruction CLRWDT or SLEEP is executed.
/TO=0, WDT timeout is occurred.
GP7, GP6, GP5: General purpose read/write register bit.
(*1) can be cleared by sleep instruction.
(*2) can be set by clrwdt instruction.

### 3.1.5 FSR (Register File Selection Register)

| Name | SFR Type | Addr. | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| FSR | R | 0x4 | BK[1:0] |  | FSR[5:0] |  |  |  |  |  |
| R/W Property |  |  | R/W |  |  |  |  |  |  |  |
| Initial Value |  |  | 0 | 0 | X | X | X | X | X | X |

FSR[5:0]: Select one register out of 64 registers of specific Bank.
BK[1:0]: Bank register used to select one specific bank of data memory. BK[1:0]=00b, Bank 0 is selected. $B K[1: 0]=01 \mathrm{~b}$, Bank 1 is selected. $\mathrm{BK}[1: 0]=10 \mathrm{~b}$, Bank 2 is selected. $B K[1: 0]=11 \mathrm{~b}$, Bank 3 is selected.

### 3.1.6 PortA (PortA Data Register)

| Name | SFR Type | Addr. | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| PortA | R | 0x5 | GP7 | GP6 | GP5 | GP4 | PA3 | PA2 | PA1 | PAO |
| R/W Property |  |  | R/W |  |  |  |  |  |  |  |
| Initial Value |  |  | Data latch value is $x x x x$, read value is $x x x x$ port value(PA3~PA0) |  |  |  |  |  |  |  |

While reading PortA, it will get the status of pins of PA regardless that pin is configured as input or output pin. While writing to PortA, data is written to PA's data latch.

GP7 ~ GP4: general register.

### 3.1.7 PortB (PortB Data Register)

| Name | SFR Type | Addr. | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| PortB | R | 0x6 | PB7 | PB6 | PB5 | PB4 | PB3 | PB2 | PB1 | PB0 |
| R/W Property |  |  | R/W |  |  |  |  |  |  |  |
| Initial Value |  |  | Data latch value is $x x x x x x x x$, read value is $x x x x x x x x$ port value(PB7~PB0) |  |  |  |  |  |  |  |

While reading PortB, it will get the status of pins of PB regardless that pin is configured as input or output pin.
While writing to PortB, data is written to PB's data latch.

### 3.1.8 PCON (Power Control Register)

| Name | SFR Type | Addr. | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| PCON | R | 0x8 | WDTEN | EIS | LVDEN | GP4 | LVREN | CMPEN | GP1 | GP0 |
| R/W Property |  |  |  |  |  |  |  |  |  |  |
| Initial Value |  |  | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

GP4, GP1, GP0: General read/write register bits.
CMPEN: Enable/disable Comparator.
CMPEN=1, enable comparator.
CMPEN=0, disable comparator.
LVREN: Enable/disable LVR.
LVREN=1, enable LVR.
LVREN=0, disable LVR.
LVDEN: Enable/disable LVD.
LVDEN=1, enable LVD.
LVDEN=0, disable LVD.
EIS: External interrupt select bit EIS=1, PB0 is external interrupt.

EIS=0, PBO is GPIO.
WDTEN: Enable/disable WDT.

WDTEN=1, enable WDT.
WDTEN=0, disable WDT.

### 3.1.9 BWUCON (PortB Wake-up Control Register)

| Name | SFR <br> Type | Addr. | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| BWUCON | R | 0x9 | WUPB7 | WUPB6 | WUPB5 | WUPB4 | WUPB3 | WUPB2 | WUPB1 | WUPB0 |
| R/W Property | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |  |  |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |

WUPBx: Enable/disable PBx wake-up function, $0 \leq x \leq 7$.
WUPBx=1, enable $P B x$ wake-up function.
WUPBx=0, disable $P B x$ wake-up function.

### 3.1.10 PCHBUF (High Byte of PC)

| Name | SFR Type | Addr. | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| PCHBUF | R | 0xA | - | XSPD_STP | - | - | - | GP5 | PCHBUF[1:0] |  |
| R/W Property |  | - | W | - | - | - | R/W | W |  |  |
| Initial Value |  | X | 0 | X | X | X | 0 | 00 |  |  |

PCHBUF[1:0]: Buffer of the $9^{\text {th }}$ bit, $8^{\text {th }}$ bit of PC.
GP5: General read/write register bit.
XSPD_STP: Write 1 to stop crystal 32.768 K speed-up function, write-only.

### 3.1.11 ABPLCON (PortA/PortB Pull-Low Resistor Control Register)

| Name | SFR <br> Type | Addr. | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ABPLCON | R | 0xB | /PLPB3 | /PLPB2 | /PLPB1 | /PLPB0 | /PLPA3 | /PLPA2 | /PLPA1 | /PLPA0 |
| R/W |  |  |  |  |  |  |  |  |  |  |
| R/W Property |  |  |  |  |  |  |  |  |  |  |
| Initial Value |  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  |

/PLPAx: Disable/enable PAx Pull-Low resistor, $0 \leq x \leq 3$.
/PLPAx=1, disable PAx Pull-Low resistor.
/PLPAx=0, enable PAx Pull-Low resistor.
/PLPBx: Disable/enable PBx Pull-Low resistor, $0 \leq x \leq 3$.
/PLPBx=1, disable PBx Pull-Low resistor.
$/ P L P B x=0$, enable PBx Pull-Low resistor.

### 3.1.12 BPHCON (PortB Pull-High Resistor Control Register)

| Name | SFR <br> Type | Addr. | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| BPHCON | R | 0xC | /PHPB7 | /PHPB6 | /PHPB5* | /PHPB4* | /PHPB3 | /PHPB2 | /PHPB1 | /PHPB0 |
| R/W |  |  |  |  |  |  |  |  |  |  |
| R/W Property |  |  |  |  |  |  |  |  |  | 1 |
| Initial Value | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  |  |  |

/PHPBx: Disable/enable PBx Pull-High resistor, $0 \leq x \leq 7$.
/PHPBx=1, disable PBx Pull-High resistor.
$/ \mathrm{PHPBx}=0$, enable PBx Pull-High resistor.
*Note: When PB4 and PB5 are used as crystal oscillator pads, the Pull-High resistor should not be enabled, or the oscillation may fail.

### 3.1.13 INTE (Interrupt Enable Register)

| Name | SFR Type | Addr. | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| INTE | R | 0xE | - | WDTIE | - | LVDIE | T1IE | INTIE | PBIE | T0IE |
| R/W Property |  | - | R/W | - | R/W | R/W | R/W | R/W | R/W |  |
| Initial Value |  | $X$ | 0 | $X$ | 0 | 0 | 0 | 0 | 0 |  |

TOIE: Timer0 overflow interrupt enable bit.
TOIE=1, enable Timer0 overflow interrupt.
TOIE=0, disable Timer0 overflow interrupt.
PBIE: PortB input change interrupt enable bit.
PBIE=1, enable PortB input change interrupt.
PBIE=0, disable PortB input change interrupt.
INTIE: External interrupt enable bit.
INTIE=1, enable external interrupt.
INTIE=0, disable external interrupt.
T1IE: Timer1 underflow interrupt enable bit.
T1IE=1, enable Timer1 underflow interrupt.
T1IE=0, disable Timer1 underflow interrupt.
LVDIE: Low-voltage detector interrupt enable bit.
LVDIE=1, enable low-voltage detector interrupt.
LVDIE=0, disable low-voltage detector interrupt.
WDTIE: WDT timeout interrupt enable bit.
WDTIE=1, enable WDT timeout interrupt.
WDTIE=0, disable WDT timeout interrupt.

### 3.1.14 INTF (Interrupt Flag Register)

| Name | SFR Type | Addr. | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| INTF | R | 0xF | - | WDTIF | - | LVDIF | T1IF | INTIF | PBIF | T0IF |
| R/W Property |  |  | - | R/W | - | R/W | R/W | R/W | R/W | R/W |
| Initial Value(note*) |  | X | 0 | X | 0 | 0 | 0 | 0 | 0 |  |

TOIF: Timer0 overflow interrupt flag bit.
TOIF=1, TimerO overflow interrupt is occurred.
TOIF must be clear by firmware.
PBIF: PortB input change interrupt flag bit.
PBIF=1, PortB input change interrupt is occurred.
PBIF must be clear by firmware.
INTIF: External interrupt flag bit.
INTIF=1, external interrupt is occurred.
INTIF must be clear by firmware.
T1IF: Timer1 underflow interrupt flag bit.
T1IF=1, Timer1 underflow interrupt is occurred.
T1IF must be clear by firmware.
LVDIF: Low-voltage detector interrupt flag bit.
LVDIF=1, Low-voltage detector interrupt is occurred.
LVDIF must be clear by firmware.
WDTIF: WDT timeout interrupt flag bit.
WDTIF=1, WDT timeout interrupt is occurred.
WDTIF must be clear by firmware.
Note: When corresponding INTE bit is not enabled, the read interrupt flag is 0.

### 3.2 TOMD Register

TOMD is a readable/writeable register which is only accessed by instruction TOMD / TOMDR.

| Name | SFR Type | Addr. | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| TOMD | - | - | LCKTM0 | INTEDG | TOCS | TOCE | PSOWDT | PSOSEL[2:0] |  |  |  |  |  |  |  |  |  |
| R/W Property |  |  |  |  |  |  |  |  |  | R/W |  |  |  |  |  |  |  |
| Initial Value(note*) |  | 0 | 0 | 1 | 1 | 1 | 111 |  |  |  |  |  |  |  |  |  |  |

PSOSEL[2:0]: Prescaler0 dividing rate selection. The rate depends on Prescaler0 is assigned to Timer0 or WDT. When Prescaler0 is assigned to WDT, the dividing rate is dependent on which timeout mechanism is selected.

| PSOSEL[2:0] | Dividing Rate |  |  |
| :---: | :---: | :---: | :---: |
|  | PSOWDT=0 <br> (Timer0) | PSOWDT=1 <br> (WDT Reset) | PSOWDT=1 <br> (WDT Interrupt) |
| 000 | $1: 2$ | $1: 1$ | $1: 2$ |
| 001 | $1: 4$ | $1: 2$ | $1: 4$ |
| 010 | $1: 8$ | $1: 4$ | $1: 8$ |
| 011 | $1: 16$ | $1: 8$ | $1: 16$ |
| 100 | $1: 32$ | $1: 16$ | $1: 32$ |
| 101 | $1: 64$ | $1: 32$ | $1: 64$ |
| 110 | $1: 128$ | $1: 64$ | $1: 128$ |
| 111 | $1: 256$ | $1: 128$ | $1: 256$ |

Table 3 Prescaler0 Dividing Rate
PSOWDT: Prescaler0 assignment.
PSOWDT=1, Prescaler0 is assigned to WDT.
PSOWDT=0, Prescaler0 is assigned to Timer0.
Note: Always set PSOWDT and PSOSEL[2:0] before enabling watchdog or timer interrupt, or reset or interrupt may be falsely triggered.

TOCE: Timer0 external clock edge selection.
TOCE=1, Timer0 will increase one while high-to-low transition occurs on pin EX_CKI.
TOCE=0, Timer0 will increase one while low-to-high transition occurs on pin EX_CKI.
Note: TOCE is also applied to Low Oscillator Frequency as timer0 clock source condition.
TOCS: Timer0 clock source selection.
TOCS=1, External clock on pin EX_CKI or Low Oscillator Frequency (I_LRC or E_LXT) is selected.
TOCS=0, Instruction clock Finst is selected.
INTEDG: Edge selection of external interrupt.
INTEDG=1, INTIF will be set while rising edge occurs on pin PBO.
INTEDG $=0$, INTIF will be set while falling edge occurs on pin PBO.
LCKTM0: When TOCS=1, timer 0 clock source can be optionally selected to be low-frequency oscillator.
TOCS $=0$, Instruction clock Finst is selected as timer0 clock source.
TOCS $=1$, LCKTM0 $=0$, external clock on pin EX_CKI is selected as timer0 clock source.
TOCS=1, LCKTM0=1, Low Oscillator Frequency (I_LRC or E_LXT, depends on configuration word Low Oscillator Frequency) output replaces pin EX_CKI as timer0 clock source.

Note: For more detail descriptions of timer0 clock source select, please see timer0 section.

### 3.3 F-page Special Function Register

### 3.3.1 IOSTA (PortA I/O Control Register)

| Name | SFR Type | Addr. | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| IOSTA | F | $0 \times 5$ | - | - | - | - | IOPA3 | IOPA2 | IOPA1 | IOPA0 |
| RW Property |  | - | - | - | - | R/W | RW | R/W | R/W |  |
| Initial Value |  | X | X | X | X | 1 | 1 | 1 | 1 |  |

IOPAx: PAx I/O mode selection, $0 \leq x \leq 3$.
IOPAx=1, PAx is input mode.
IOPAx=0, PAx is output mode.

### 3.3.2 IOSTB (PortB I/O Control Register)

| Name | SFR Type | Addr. | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| IOSTB | F | 0x6 | IOPB7 | IOPB6 | IOPB5 | IOPB4 | IOPB3 | IOPB2 | IOPB1 | IOPB0 |
| R/W Property |  | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |  |
| Initial Value | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  |  |

IOPBx: PBx I/O mode selection, $0 \leq x \leq 7$.
$I O P B x=1, P B x$ is input mode.
$1 O P B x=0, P B x$ is output mode.

### 3.3.3 PSOCV (Prescaler0 Counter Value Register)

| Name | SFR Type | Addr. | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| PSOCV | F | 0xA | PSOCV[7:0] |  |  |  |  |  |  |  |
| RW Property |  |  | R |  |  |  |  |  |  |  |
| Initial Value |  |  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

While reading PSOCV, it will get current value of Prescaler0 counter.

### 3.3.4 BODCON (PortB Open-Drain Control Register)

| Name | SFR <br> Type | Addr. | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| BODCON | F | 0xC | ODPB7 | ODPB6 | ODPB5 | ODPB4 | GP3 | ODPB2 | ODPB1 | ODPB0 |
| RW Property |  |  |  |  |  |  |  |  | R/W |  |
| Initial Value |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |

ODPBx: Enable/disable open-drain of $\mathrm{PBx}, \mathrm{x}=0,1,2,4,5,6,7$.
ODPBx=1, enable open-drain of PBx.
$O D P B x=0$, disable open-drain of $P B x$.

GP3: General purpose register bit.

### 3.3.5 CMPCR (Comparator voltage select Control Register)

| Name | SFR Type | Addr. | Bit7 | Bit6 | Bit5 |  | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| CMPCR | F | 0xE | GP7 | RBIAS_H | RBIAS_L |  | CMPF_INV | PS1 | PSO | NS1 | NSO |
| R/W Property |  |  | R/W |  |  |  |  |  |  |  |  |
| Initial Value |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  | 0 |

NS[1:0]: Comparator inverting input select.

| NS[1:0] | Inverting input |
| :---: | :---: |
| 00 | PA1 |
| 01 | PA3 |
| 10 | Bandgap $(0.65 \mathrm{~V})$ |
| 11 | Vref |

PS[1:0]: Comparator non-inverting input select

| PS[1:0] | Non-inverting input |
| :---: | :---: |
| 00 | PA0 |
| 01 | PA2 |
| 10 | Vref |
| 11 | --- |

CMPF_INV: Comparator output inverse control bit.
CMPF_INV = 1, Inverse comparator output.
CMPF_INV $=0$, Non-inverse comparator output.
RBIAS_L, RBIAS_H: Set corresponding voltage reference levels
(please refer to chapter 3.11.1)
Note: RBIAS_L and RBIAS_H MUST be set as " 00 " before sleep mode or halt mode to prevent current leakage.

### 3.3.6 PCON1 (Power Control Register1)

| Name | SFR Type | Addr. | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| PCON1 | F | 0xF | GIE | LVDOUT | LVDS3 | LVDS2 | LVDS1 | LVDS0 | GP1 | TOEN |
| R/W Property |  | R/W ${ }^{\left(1^{*}\right)}$ | R | R/W | R/W | R/W | R/W | R/W | R/W |  |
| Initial Value |  | 0 | X | 1 | 1 | 1 | 1 | 0 | 1 |  |

TOEN: Enable/disable Timer0.

TOEN=1, enable Timer0.
TOEN=0, disable Timer0.
LVDS3~0: Select one of the 14 LVD voltage.

| LVDS[3:0] | Voltage |
| :---: | :---: |
| 0000 | --- |
| 0001 | --- |
| 0010 | 2.2 V |
| 0011 | 2.4 V |
| 0100 | 2.6 V |
| 0101 | 2.8 V |
| 0110 | 2.9 V |
| 0111 | 3.0 V |
| 1000 | 3.15 V |
| 1001 | 3.30 V |
| 1010 | 3.45 V |
| 1011 | 3.60 V |
| 1100 | 3.75 V |
| 1101 | 3.90 V |
| 1110 | 4.05 V |
| 1111 | 4.15 V |

Table 4 LVD voltage select
LVDOUT: Low voltage detector output, read-only.
GIE: Global interrupt enable bit.
$\mathrm{GIE}=1$, enable all unmasked interrupts.
$\mathrm{GIE}=0$, disable all interrupts.
GP1: General purpose read/write register.
(1*) : set by instruction ENI, clear by instruction DISI, read by instruction IOSTR.

### 3.4 S-page Special Function Register

### 3.4.1 TMR1 (Timer1 Register)

| Name | SFR Type | Addr. | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| TMR1 | S | $0 \times 0$ | TMR1[7:0] |  |  |  |  |  |  |  |
| R/W Property |  |  | RXXXXXXX |  |  |  |  |  |  |  |
| Initial Value |  |  |  |  |  |  |  |  |  |  |

When reading register TMR1, it will obtain current value of 8-bit down-count Timer1. When writing register TMR1, it will both write data to timer1 reload register and update Timer1 current content.

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### 3.4.2 T1CR1 (Timer1 Control Register1)

| Name | SFR Type | Addr. | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| T1CR1 | S | $0 \times 1$ | PWM1OEN | PWM1OAL | - | - | - | T1OS | T1RL | T1EN |
| RW Property |  | W | W | - | - | - | R/W | R/W | R/W |  |
| Initial Value |  | 0 | 0 | X | X | X | 0 | 0 | 0 |  |

This register is used to configure Timer1 functionality.
T1EN: Enable/disable Timer1.
T1EN=1, enable Timer1.
T1EN=0, disable Timer1.
T1RL: Configure Timer1 down-count mechanism while Non-Stop mode is selected (T1OS=0).
T1RL=1, initial value is reloaded from reload register TMR1.
T1RL=0, continuous down-count from 0xFF when underflow is occurred.
T10S: Configure Timer1 operating mode while underflow is reached.
T1OS $=1$, One-Shot mode. Timer1 will count once from the initial value to $0 \times 00$.
T1OS=0, Non-Stop mode. Timer1 will keep down-count after underflow.

| T10S | T1RL | Timer1 Down-Count Functionality |
| :---: | :---: | :--- |
| 0 | 0 | Timer1 will count from reload value down to 0x00. <br> When underflow is reached, $0 x F F$ <br> is reloaded and continues down-count. |
| 0 | 1 | Timer1 will count from reload value down to 0x00. <br> When underflow is reached, reload value is reloaded and continues to down-count. |
| 1 | x | Timer1 will count from initial value down to $0 \times 00$. <br> When underflow is reached, Timer1 will stop down-count. |

Table 5 Timer1 Functionality
PWM1OAL: Define PWM1 output active state.
PWM1OAL=1, PWM1 output is active low.
PWM1OAL=0, PWM1 output is active high.
PWM10EN: Enable/disable PWM1 output.
PWM1OEN=1, PWM1 output will be present on PB6 or PB2.
$\mathrm{PWM} 10 E \mathrm{~N}=0, \mathrm{~PB} 6$ or PB 2 is GPIO.

### 3.4.3 T1CR2 (Timer1 Control Register2)

| Name | SFR Type | Addr. | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| T1CR2 | S | $0 \times 2$ | - | - | T1CS | T1CE | /PS1EN | PS1SEL[2:0] |  |  |


| R/W Property | - | - | $R / W$ | $R / W$ | $R / W$ | $R / W$ | $R / W$ | $R / W$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Initial Value | X | X | 1 | 1 | 1 | 1 | 1 | 1 |

This register is used to configure Timer1 functionality.
PS1SEL[2:0]: Prescaler1 dividing rate selection.

| PS1SEL[2:0] | Dividing Rate |
| :---: | :---: |
| 000 | $1: 2$ |
| 001 | $1: 4$ |
| 010 | $1: 8$ |
| 011 | $1: 16$ |
| 100 | $1: 32$ |
| 101 | $1: 128$ |
| 110 | $1: 256$ |
| 111 |  |

Table 6 Prescaler1 Dividing Rate

## Note: Always set PS1SEL[2:0] at /PS1EN=1, or interrupt may be falsely triggered.

/PS1EN: Disable/enable Prescaler1.
/PS1EN=1, disable Prescaler1.
/PS1EN=0, enable Prescaler1.
T1CE: Timer1 external clock edge selection.
T1CE=1, Timer1 will decrease one while high-to-low transition occurs on pin EX_CKI.
T1CE=0, Timer1 will decrease one while low-to-high transition occurs on pin EX_CKI.
T1CS: Timer1 clock source selection.
T1CS=1, External clock on pin EX_CKI is selected.
T1CS=0, Instruction clock is selected.

### 3.4.4 PWM1DUTY (PWM1 Duty Register)

| Name | SFR Type | Addr. | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| PWM1DUTY | S | 0x3 | PWM1DUTY[7:0] |  |  |  |  |  |  |  |
| R/W Property |  |  | W |  |  |  |  |  |  |  |
| Initial Value |  |  | XXXXXXXX |  |  |  |  |  |  |  |

This register is write-only. After Timer1 is enabled and start down-count, PWM1 output will keep at inactive state. While Timer1 value is equal to PWM1DUTY, PWM1 output will become active state until underflow is occurred.

Moreover, the reload value of Timer1 stored on register TMR1 is used to define the PWM1 frame rate and register PWM1DUTY is used to define the duty cycle of PWM1.

### 3.4.5 PS1CV (Prescaler1 Counter Value Register)

| Name | SFR Type | Addr. | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| PS1CV | S | 0x4 | PS1CV[7:0] |  |  |  |  |  |  |  |
| R/W Property |  |  | R |  |  |  |  |  |  |  |
| Initial Value |  |  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

While reading PS1CV, it will get current value of Prescaler1 counter.

### 3.4.6 BZ1CR (Buzzer1 Control Register)

| Name | SFR Type | Addr. | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| BZ1CR | S | $0 \times 5$ | BZ1EN | - | - | - | BZ1FSEL[3:0] |  |  |  |  |
| RW Property |  | W | - | - | - | W |  |  |  |  |  |
| Initial Value |  | 0 | X | X | X | 1 | 1 | 1 | 1 |  |  |

BZ1FSEL[3:0]: Frequency selection of BZ1 output.

| BZ1FSEL[3:0] | BZ1 Frequency Selection |  |
| :---: | :---: | :---: |
|  | Clock Source | Dividing Rate |
| 0000 | Prescaler1 output | 1:2 |
| 0001 |  | 1:4 |
| 0010 |  | 1:8 |
| 0011 |  | 1:16 |
| 0100 |  | 1:32 |
| 0101 |  | 1:64 |
| 0110 |  | 1:128 |
| 0111 |  | 1:256 |
| 1000 | Timer1 output | Timer1 bit 0 |
| 1001 |  | Timer1 bit 1 |
| 1010 |  | Timer1 bit 2 |
| 1011 |  | Timer1 bit 3 |
| 1100 |  | Timer1 bit 4 |
| 1101 |  | Timer1 bit 5 |
| 1110 |  | Timer 1 bit 6 |
| 1111 |  | Timer 1 bit 7 |

Table 7 Buzzer1 Output Frequency Selection

BZ1EN: Enable/Disable BZ1 output.
BZ1EN=1, enable Buzzer1.
BZ1EN=0, disable Buzzer1.

### 3.4.7 IRCR (IR Control Register)

| Name | SFR Type | Addr. | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| IRCR | S | $0 \times 6$ | IROSC358M | - | - | - | - | IRCSEL | IRF57K | IREN |
| R/W Property |  | W | - | - | - | - | W | W | W |  |
| Initial Value |  | 0 | $\times$ | $\times$ | $\times$ | X | 0 | 0 | 0 |  |

IREN: Enable/Disable IR carrier output.
IREN=1, enable IR carrier output.
IREN=0, disable IR carrier output.
IRF57K: Selection of IR carrier frequency.
IRF57K=1, IR carrier frequency is 57 KHz .
IRF57K=0, IR carrier frequency is 38 KHz .

IRCSEL: Polarity selection of IR carrier.
$\operatorname{IRCSEL}=0, \operatorname{IR}$ carrier will be generated when I/O pin data is 1 .
IRCSEL=1, IR carrier will be generated when I/O pin data is 0 .
IROSC358M: When external crystal is used, this bit is determined according to what kind of crystal is used.
This bit is ignored if internal high frequency oscillation is used.
IROSC358M=1, crystal frequency is 3.58 MHz .
IROSC358M=0, crystal frequency is 455 KHz .

## Note:

1. Only high oscillation (FHosc) (See section 3.14) can be used as IR clock source.

## 2. Division ratio for different oscillation type.

| OSC. Type | $\mathbf{5 7 K H z}$ | $\mathbf{3 8 K H z}$ | Conditions |
| :---: | :---: | :---: | :--- |
| High IRC(4MHz) | 64 | 96 | HIRC mode (the input to IR module is set to 4MHz no matter <br> what system clock is) |
| Xtal 3.58MHz | 64 | 96 | Xtal mode \& IROSC358M=1 |
| Xtal 455KHz | 8 | 12 | Xtal mode \& IROSC358M $=0$ |

Table 8 Division ratio for different oscillation type

### 3.4.8 TBHP (Table Access High Byte Address Pointer Register)

| Name | SFR Type | Addr. | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| TBHP | S | $0 \times 7$ | - | - | - | - | - | TBHP2 | TBHP1 | TBHP0 |
| R/W Property |  | - | - | - | - | - | R/W | R/W | R/W |  |
| Initial Value |  | $\times$ | $\times$ | $\times$ | $\times$ | $X$ | $\times$ | X | X |  |

When instruction CALLA, GOTOA or TABLEA is executed, the target address is constituted by TBHP[2:0] and ACC. ACC is the Low Byte of PC[9:0] and TBHP[1:0] is the high byte of PC[9:0]. TBHP[2] is general register for NY8A053E.

### 3.4.9 TBHD (Table Access High Byte Data Register)

| Name | SFR Type | Addr. | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| TBHD | S | 0x8 | - | - | TBHD5 | TBHD4 | TBHD3 | TBHD2 | TBHD1 | TBHD0 |
| R/W Property |  | - | - | R | R | R | R | R | R |  |
| Initial Value |  | X | X | X | X | X | X | X | X |  |

When instruction TABLEA is executed, high byte of content of addressed ROM is loaded into TBHD[5:0] register. The Low Byte of content of addressed ROM is loaded to ACC.

### 3.4.10 P2CR1 (PWM2 Control Register1)

| Name | SFR Type | Addr. | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| P2CR1 | S | 0xA | PWM2OEN | PWM2OAL | - | - | - | - | - | - |
| R/W Property |  | R/W | R/W | - | - | - | - | - | - |  |
| Initial Value |  | 0 | 0 | X | X | X | X | X | X |  |

PWM2OAL: Define PWM2 output active state.
$P W M 2 O A L=1, P W M 2$ output is active low.
PWM2OAL=0, PWM2 output is active high.
PWM2OEN: Enable/disable PWM2 output.
PWM2OEN=1, PWM2 output will be present on PA1 or PA0.
PWM2OEN $=0$, PA1 or PA0 is GPIO.

### 3.4.11 PWM2DUTY (PWM2 Duty Register)

| Name | SFR Type | Addr. | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| PWM2DUTY | S | 0xC | PWM2DUTY[7:0] |  |  |  |  |  |  |  |
| R/W Property |  |  | W |  |  |  |  |  |  |  |
| Initial Value |  |  | XXXXXXXX |  |  |  |  |  |  |  |

The reload value of 10-bit Timer1 stored on registers TMRH[5:4] and TMR1[7:0] is used to define the PWM2 frame rate, and registers TMRH[3:2] and PWM2DUTY[7:0] is used to define the duty cycle of PWM2.

### 3.4.12 TMRH (Timer High Byte Register)

| Name | SFR <br> Type | Addr. | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| TMRH | S | 0xD | - | - | TMR19 | TMR18 | PWM2 <br> DUTY9 | PWM2 <br> DUTY8 | PWM1 <br> DUTY9 | PWM1 <br> DUTY8 |
| R/W Property |  | - | - | R/W | R/W | R/W | R/W | R/W | R/W |  |
| Initial Value |  | X | X | X | X | X | X | X | X |  |

TMR19~8: Timer1 MSB 2 bits. Write these 2 bits will overwrite the 10 -bit Timer1 load value of bit 9 and 8.
Read these 2 bits will get the Timer1 bit9-8 current value.
PWM2DUTY9~8: PWM2 duty data MSB 2 bits.
PWM1DUTY9~8: PWM1 duty data MSB 2 bits.

### 3.4.13 TM34RH (Timer3 High Byte Register)

| Name | SFR <br> Type | Addr. | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| TM34RH | S | 0xE | - | - | - | - | PWM4 <br> DUTY9 | PWM4 <br> DUTY8 | PWM3 <br> DUTY9 | PWM3 <br> DUTY8 |
| R/W Property |  | - | - | - | - | R/W | R/W | R/W | R/W |  |
| Initial Value |  | $X$ | $X$ | $X$ | $X$ | $X$ | $X$ | $X$ | $X$ |  |

PWM3DUTY9~8: PWM3 duty data MSB 2 bits.
PWM4DUTY9~8: PWM4 duty data MSB 2 bits.

### 3.4.14 OSCCR (Oscillation Control Register)

| Name | SFR Type | Addr. | Bit7 | Bit6 | Bit <br> $\mathbf{5}$ | Bit <br> $\mathbf{4}$ | Bit3 | Bit2 | Bit1 | Bit0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| OSCCR | S | $0 \times F$ | - | CMPOEN | - | - | OPMD[1:0] | STPHOSC | SELHOSC |  |
| R/W Property |  | - | R/W | - | - | R/W | R/W | R/W |  |  |
| Initial Value |  |  | $X$ | 0 | $X$ | $X$ | 00 | 0 | 1 |  |

SELHOSC: Selection of system oscillation (Fosc).
SELHOSC=1, Fosc is high-frequency oscillation (Fноsc).
SELHOSC=0, Fosc is low-frequency oscillation (Flosc).
STPHOSC: Disable/enable high-frequency oscillation (Fhosc).
STPHOSC=1, Fhosc will stop oscillation and be disabled.
STPHOSC=0, Fhosc keep oscillation.
OPMD[1:0]: Selection of operating mode.

| OPMD[1:0] | Operating Mode |
| :---: | :---: |
| 00 | Normal mode |
| 01 | Halt mode |


| OPMD[1:0] | Operating Mode |
| :---: | :---: |
| 10 | Standby mode |
| 11 | reserved |

## Table 9 Selection of Operating Mode by OPMD[1:0]

Note: STPHOSC cannot be changed with SELHOSC or OPMD at the same time. STPHOSC cannot be changed with OPMD at the same time during SELHOSC=1.

CMPOEN: Enable/Disable comparator output to pad PB1.
CMPOEN=1, Enable comparator output to pad PB1.
CMPOEN=0, Disable comparator output to pad PB1.
Note: Comparator output to pad PB1 has higher priority than PWM3/IR.

### 3.4.15 P3CR1 (PWM3 Control Register1)

| Name | SFR Type | Addr. | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| P3CR1 | S | 0x11 | PWM3OEN | PWM3OAL | - | - | - | - | - | - |
| R/W Property |  | R/W | R/W | - | - | - | - | - | - |  |
| Initial Value |  | 0 | 0 | $X$ | $X$ | X | X | $X$ | $X$ |  |

PWM3OAL: Define PWM3 output active state.
PWM3OAL=1, PWM3 output is active low.
PWM3OAL=0, PWM3 output is active high.
PWM30EN: Enable/disable PWM3 output.
PWM3OEN=1, PWM3 output will be present on PA3 or PB1.
PWM3OEN $=0$, PA3 or PB1 is GPIO.

### 3.4.16 PWM3DUTY (PWM3 Duty Register)

| Name | SFR Type | Addr. | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| PWM3DUTY | S | 0x13 | PWM3DUTY[7:0] |  |  |  |  |  |  |  |
| R/W Property |  |  | W |  |  |  |  |  |  |  |
| Initial Value |  |  | XXXXXXXX |  |  |  |  |  |  |  |

The reload value of 10-bit Timer1 stored on registers TMRH[5:4] and TMR1[7:0] is used to define the PWM3 frame rate, and registers TM34RH[1:0] and PWM3DUTY[7:0] is used to define the duty cycle of PWM3.

### 3.4.17 P4CR1 (PWM4 Control Register1)

| Name | SFR Type | Addr. | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| P4CR1 | S | $0 \times 16$ | PWM4OEN | PWM4OAL | - |  | - | - | - | - |
| R/W Property |  | R/W | R/W | - | - | - | - | - | - |  |
| Initial Value |  | 0 | 0 | X | X | X | X | X | X |  |

PWM40AL: Define PWM4 output active state.
PWM4OAL=1, PWM4 output is active low.
PWM4OAL=0, PWM4 output is active high.
PWM4OEN: Enable/disable PWM4 output.
PWM4OEN=1, PWM4 output will be present on PA2 or PB0.
PWM4OEN=0, PA2 or PB0 is GPIO.

### 3.4.18 PWM4DUTY (PWM4 Duty Register)

| Name | SFR Type | Addr. | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| PWM4DUTY | S | 0x18 | PWM4DUTY[7:0] |  |  |  |  |  |  |  |
| R/W Property |  |  | W |  |  |  |  |  |  |  |
| Initial Value |  |  | XXXXXXXX |  |  |  |  |  |  |  |

The reload value of 10-bit Timer1 stored on registers TMRH[5:4] and TMR1[7:0] is used to define the PWM4 frame rate, and registers TM34RH[3:2] and PWM4DUTY[7:0] is used to define the duty cycle of PWM4.

### 3.5 I/O Port

NY8A053E provides $12 \mathrm{I} / \mathrm{O}$ pins which are PA[3:0] and $\mathrm{PB}[7: 0]$. User can read/write these $\mathrm{I} / \mathrm{O}$ pins through registers PORTA and PORTB respectively. Each I/O pin has a corresponding register bit to define it is input pin or output pin. Register IOSTA[3:0] define the input/output direction of PA[3:0]. Register IOSTB[7:0] define the input/output direction of PB[7:0].

When an I/O pin is configured as input pin, it may have Pull-High resistor or Pull-Low resistor which is enabled or disabled through registers. Register ABPLCON[3:0] are used to enable or disable Pull-Low resistor of PA[3:0]. Register BPHCON[7:0] are used to enable or disable Pull-High resistor of $\mathrm{PB}[7: 0]$. Register ABPLCON[7:4] are used to enable or disable Pull-Low resistor of $\mathrm{PB}[3: 0]$.

When an I/O pin is configured as output pin, there is a corresponding and individual register to select as Open-Drain output pin. Register BODCON[7:0] determine PB[7:0] is Open-Drain or not. (Except PB[3], which is always in open-drain mode when configured as output port.)

The summary of Pad I/O feature is listed in the table below.

| Feature |  | PA[3:0] | $\mathrm{PB}[2: 0]$ | $\mathrm{PB}[3]$ | $\mathrm{PB}[7: 4]$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Input | Pull-High Resistor | X | V | V | V |
|  | Pull-Low Resistor | V | V | V | X |
| Output | Open-Drain | X | V | always | V |

Table 10 Summary of Pad I/O Feature
The level change on each I/O pin of PB may generate interrupt request. Register BWUCON[7:0] will select which I/O pin of PB may generate this interrupt. As long as any pin of PB is selected by corresponding bit of BWUCON, the register bit PBIF (INTF[1]) will set to 1 if there is a level change occurred on any selected pin. An interrupt request will occur and interrupt service routine will be executed if register bit PBIE (INTE[1]) and GIE (PCON1[7]) are both set to 1.

There is one external interrupt provided by NY8A053E. When register bit EIS (PCON[6]) is set to 1, PB0 is used as input pin for external interrupt.

Note: When PBO is both set as level change operation and external interrupt, the external interrupt will have higher priority, and the PB0 level change operation will be disabled. But PB7~PB1 level change function are not affected.

NY8A053E can provide IR carrier generation. IR carrier generation is enabled by register bit IREN (IRCR[0]) and carrier will be present on a PB1 pin. Configuration word IR Current determines sink current value of IR carrier.

PB3 can be used as external reset input determined by a configuration word. When an active-low signal is applied to PB3, it will cause NY8A053E to enter reset process.

When external crystal ( E _HXT, E _XT or E _LXT) is adopted for high oscillation or low oscillation according to setting of configuration words, PB5 will be used as crystal input pin (Xin) and PB4 will be used as crystal output pin (Xout).

When I_HRC or I_LRC mode is selected as system oscillation and E_HXT, E_XT or E_LXT is not adopted, instruction clock is observable on PB4 if a configuration word is enabled.

Moreover, PB2 can be timer 0 external clock source EX_CKI if TOMD TOCS=1 and LCK_TM0=0. PB2 can be timer 1 external clock source if $\mathrm{T} 1 \mathrm{CS}=1$.

Moreover, PB6 or PB2 can be PWM1 output and PB7 or PB2 can be Buzzer1 output. If T1CR1[7] PWM1OEN=1, PB6 or PB2 can be PWM1 output. And if BZ1CR[7] BZ1EN=1, PB7 or BP2 can be Buzzer1 output.

### 3.5.1 Block Diagram of IO Pins

IO_SEL:
WRITE_EN: write data to pad.
READ EN:
PULLDOWN_EN:
RD_TYPE : select read pin or read latch.


Figure 5 Block Diagram of PA[3:0]

OD_EN: open-drain enable.
IO_SEL: set pad input or output.
WRITE_EN: write data to pad.
READ_EN: read pad to DATA_BUS.
PULLDOWN_EN: enable Pull-Low.
PULLUP_ENB: enable pull high.

## WUBx: wake-up enable.

INTEDGE: external interrupt edge select
SET_PBIF: set port change interrupt flag.
RD_TYPE: select read pin or read latch.


Figure 6 Block Diagram of PB0

OD_EN: open-drain enable.
IREN: Enable IR.
IO_SEL: set pad input or output.
WRITE_EN: write data to pad.
READ_EN: read pad to DATA_BUS.
PULLDOWN_EN: enable Pull-Low.
PULLUP_ENB: enable pull high.
WUBx: wake-up enable.
RD_TYPE: read pin or read latch.
SET_PBIF: set port change interrupt flag.


Figure 7 Block Diagram of PB1

OD_EN: open-drain enable.
IO_SEL: set pad input or output.
WRITE_EN: write data to pad.
READ_EN: read pad to DATA_BUS.
PULLDOWN_EN: enable Pull-Low.
PULLUP_ENB: enable pull high.
WUBx: wake-up enable.
SET_PBIF: set port change interrupt flag.
RD_TYPE: read pin or read latch.
EX_CKI: Timer0 EX CLOCK IN.


Figure 8 Block Diagram of PB2

PB3_RSTPAD: PB3 is set as Reset Pin by configuration word.
IO_SEL: set pad input or output.
WRITE_EN: write data to pad.
READ_EN: read pad to DATA_BUS.
PULLDOWN_EN: enable Pull-Low.
PULLUP_ENB: enable pull high.
WUBx: wake-up enable.
SET_PBIF: set port change interrupt flag.
RD_TYPE: read pin or read latch.
RSTB_IN: $\quad$ Reset signal with Schmitt trigger.


Figure 9 Block Diagram of PB3

OD_EN: open-drain enable.
XTL_EN: PB4, PB5 is set as Xtal Pin by configuration word.
IO_SEL: set pad input or output.
WRITE_EN: write data to pad.
READ_EN: read pad to DATA_BUS.
PULLUP_ENB: enable pull high.
WUBx: wake-up enable.
RD_TYPE: read pin or read latch
SET_PBIF: set port change interrupt flag.


Figure 10 Block Diagram of PB5, PB4

OD_EN: open-drain enable.
DATA_BUS: PWM or Buzzer data.
IO_SEL: set pad input or output.
WRITE_EN: write data to pad.
READ_EN: read pad to DATA_BUS.
PULLUP_ENB: enable pull high.
WUB: wake-up enable.
RD_TYPE: read pin or read latch.
SET_PBIF: set port change interrupt flag.


Figure 11 Block Diagram of PB7, PB6

### 3.6 Timer0

Timer0 is an 8-bit up-count timer and its operation is enabled by register bit TOEN (PCON1[0]). Writing to Timer0 will set its initial value. Reading from Timer0 will show its current count value.

The clock source to Timer0 can be from instruction clock, external pin EX_CKI or low speed clock Low Oscillator Frequency according to register bit TOCS and LCK_TM0 (TOMD[5] and TOMD[7]). When TOCS is 0, instruction clock is selected as Timer0 clock source. When TOCS is 1 and LCK_TMO is 0 , EX_CKI is selected as Timer0 clock source. When TOCS is 1 and LCK_TM0 is 1 (and Timer0 source must set to 1), Low Oscillator Frequency (I_LRC or E_LXT, depends on configuration word) output is selected. Summarized table is shown below. (Also check Figure. 12)

| Timer0 clock source | TOCS | LCKTMO | Timer0 source | Low Oscillator <br> Frequency |
| :---: | :---: | :---: | :---: | :---: |
| Instruction clock | 0 | X | X | X |
| EX_CKI | 1 | 0 | X | X |
|  |  | X | 0 | X |
| E_LXT | 1 | 1 | 1 | 1 |
| I_LRC | 1 | 1 | 1 | 0 |

Table 11 Summary of Timer0 clock source control
Moreover the active edge of EX_CKI or Low Oscillator Frequency to increase Timer0 can be selected by register bit TOCE (TOMD[4]). When TOCE is 1, high-to-low transition on EX_CKI or Low Oscillator Frequency will increase Timer0. When TOCE is 0 , low-to-high transition on EX_CKI or Low Oscillator Frequency will increase Timer0. When using Low Oscillator Frequency as timer0 clock source, it is suggested to use prescaler0 (see below descriptions) and the ratio set to more than 4, or missing count may happen.

Before Timer0 clock source is supplied to Timer0, it can be divided by Prescaler0 if register bit PSOWDT (TOMD[3]) is clear to 0 . When writing 0 to PSOWDT by instruction, Prescaler0 is assigned to Timer0 and Prescaler0 will be clear after this instruction is executed. The dividing rate of Prescaler0 is determined by register bits PSOSEL[2:0] which is from 1:2 to 1:256.

When Timer0 is overflow, the register bit TOIF (INTF[0]) will be set to 1 to indicate Timer0 overflow event is occurred. If register bit TOIE (INTE[0]) and GIE are both set to 1 , interrupt request will occur and interrupt service routine will be executed. TOIF will not be clear until firmware writes 0 to TOIF.

The block diagram of Timer0 and WDT is shown in the figure below.


Figure 12 Block Diagram of Timer0 and WDT

### 3.7 Timer1/PWM1/Buzzer1

Timer1 is an 10-bit down-count timer with Prescaler1 whose dividing rate is programmable. The output of Timer1 can be used to generate PWM1 output and Buzzer1 output. A write to the Timer1 will both write to a timer1 reload register (T1rld) and timer1 counter. A read to the timer1 will show the content of the Timer1 current count value.

The block diagram of Timer1 is shown in the figure below.


Figure 13 Block Diagram of Timer1
The operation of Timer1 can be enabled or disabled by register bit T1EN (T1CR1[0]). After Timer1 is enabled, its clock source can be instruction clock or pin EX_CKI which is determined by register bit T1CS (T1CR2[5]). When T1CS is 1, EX_CKI is selected as clock source. When T1CS is 0 , instruction clock is selected as clock source. When EX_CKI is selected, the active edge to decrease Timer1 is determined by register bit T1CE (T1CR2[4]). When T1CE is 1 , high-to-low transition on EX_CKI will decrease Timer1. When T1CE is 0 , low-to-high transition
on EX_CKI will decrease Timer1. The selected clock source can be divided further by Prescaler1 before it is applied to Timer1. Prescaler1 is enabled by writing 0 to register bit /PS1EN (T1CR2[3]) and the dividing rate is from 1:2 to 1:256 determined by register bits PS1SEL[2:0] (T1CR2[2:0]). Current value of Prescaler1 can be obtained by reading register PS1CV.

Timer1 provide two kinds of operating mode: one is One-Shot mode and the other is Non-Stop mode. When register bit T1OS (T1CR1[2]) is 1, One-Shot mode is selected. Timer1 will count down once from initial value stored on register TMR1 to 0x00, i.e. underflow is occurred. When register bit T1OS (T1CR1[2]) is 0, Non-Stop mode is selected. When underflow is occurred, there are two selections to start next down-count which is determined by register bit T1RL (T1CR1[1]). When T1RL is 1, the initial value stored on register TMR1 will be restored and start next down-count from this initial value. When T1RL is 0, Timer1 will start next down-count from $0 x F F$.

When Timer1 is underflow, the register bit T1IF (INTF[3]) will be set to 1 to indicate Timer1 underflow event is occurred. If register bit T1IE (INTE[3]) and GIE are both set to 1, interrupt request will occur and interrupt service routine will be executed. T1IF will not be clear until firmware writes 0 to T1IF.

The timing chart of Timer1 is shown in the following figure.


Figure 14 Timer1 Timing Chart
The PWM1 output can be available on I/O pin PB2 or PB6 when register bit PWM1OEN (T1CR1[7]) is set to 1. Moreover, PB2 or PB6 will become output pin automatically. The active state of PWM1 output is determined by register bit PWM1OAL (T1CR1[6]). When PWM1OAL is 1, PWM1 output is active low. When PWM1OAL is 0, PWM1 output is active high. Moreover, the duty cycle and frame rate of PWM1 are both programmable. The duty cycle is determined by registers TMRH[1:0] and PWM1DUTY[7:0]. When PWM1DUTY is 0, PWM1 output will be never active. When PWM1DUTY is $0 \times 3 F F$, PWM1 output will be active for 1023 Timer1 input clocks. The frame rate is determined by TMRH[5:4] + TMR1[7:0] initial value. Therefore, PWM1DUTY value must be less than or equal to TMRH[5:4] + TMR1[7:0]. When user write PWM1DUTY, write PWM1DUTY[9:8] MSB 2
bits(TMRH[1:0]) first and write PWM1DUTY[7:0] second, PWM1 duty register will be updated after Timer1 overflow occurs. The block diagram of PWM1 is illustrated in the following figure.


Figure 15 PWM1 Block Diagram

The Buzzer1 output (BZ1) can be available on I/O pin PB7 or PB2 when register bit BZ1EN (BZ1CR1[7]) is set to 1 . Moreover, PB7 or PB2 will become output pin automatically. The frequency of BZ1 can be derived from Timer1 output or Prescaler1 output and dividing rate is determined by register bits BZ1FSEL[3:0] (BZ1CR[3:0]). When BZ1FSEL[3] is 0, Prescaler1 output is selected to generate BZ1 output. When BZ1FSEL[3] is 1, Timer1 output is selected to generate BZ1 output. The dividing rate can be from 1:2 to 1:256 in order to generate all kinds of frequency. The block diagram of Buzzer1 is illustrated in the following figure.


Figure 16 Buzzer1 Block Diagram

### 3.8 PWM2/3/4

The PWM2/3/4 output can be available on PortA or PortB when register bit PWMxOEN $(x=2,3,4)$ is set to 1. Moreover, PortA or PortB will become output pin automatically. The active state of PWM2/3/4 output is determined by register bit PWMxOAL. When PWMxOAL is 1 , PWM2/3/4 output is active low. When PWMxOAL is $0, \mathrm{PWM} 2 / 3 / 4$ output is active high. Moreover, the duty cycle and frame rate of $\mathrm{PWM} 2 / 3 / 4$ are both
programmable. The duty cycle is determined by register PWMxDUTY. When PWMxDUTY is 0 , PWM2/3/4 output will be never active. When PWMxDUTY is $0 \times 3 F F$, PWM2/3/4 output will be active for 1023 Timer1 input clocks. The frame rate is determined by TMRH[5:4], TMR1[7:0] initial value. Therefore, PWMxDUTY value must be less than or equal to TMR1[9:0]. Besides, user needs to set P2CR1 because PWM2/3/4 are both shared with Timer1. When user write PWMxDUTY, write PWMxDUTY[9:8] MSB 2 bits first and write PWMxDUTY[7:0] second, PWM2/3/4 duty register will be updated after Timer1 overflow occurs. The block diagram of PWM2/3/4 is illustrated in the following figure.


Figure 17 PWM2/3/4 Block Diagram

### 3.9 IR Carrier

The IR carrier will be generated after register bit IREN (IRCR[0]) is set to 1 . Moreover, PB1 will become output pin automatically. When IREN is clear to 0, PB1 will become general I/O pin as it was configured.

The IR carrier frequency is selectable by register bit IRF57K (IRCR[1]). When IRF57K is 1, IR carrier frequency is 57 KHz . When IRF57K is 0 , IR carrier frequency is 38 KHz . Because IR carrier frequency is derived from high frequency system oscillation Fhosc, it is necessary to specify what frequency is used as system oscillation when external crystal is used. Register bit IROSC358M (IRCR[7]) is used to provide NY8A053E this information. When IROSC358M is 1 , frequency of external crystal is 3.58 MHz and when IROSC358M is 0 , frequency of external crystal is 455 KHz . When internal high frequency oscillation is adopted, this register will be ignored, and it will provide 4 MHz clock to IR module.

The active state (polarity) of IR carrier is selectable according to PB1 output data. When register bit IRCSEL (IRCR[2]) is 1, IR carrier will be present on pin PB1 when its output data is 0 . When register bit IRCSEL (IRCR[2]) is 0 , IR carrier will be present on pin PB1 when its output data is 1 . The polarity of IR carrier is shown in the following figure.


Figure 18 Polarity of IR Carrier vs. Output Data

### 3.10 Low VoItage Detector (LVD)

NY8A053E low voltage detector (LVD) built-in precise band-gap reference for accurately detecting $V_{d o}$ level. If LVDEN (register PCON[5]) $=1$ and VDD voltage value falls below LVD voltage which is selected by LVDS[3:0] as table shown below, the LVD output will become low. If the LVD interrupt is enabled, the LVD interrupt flag will be high and if GIE=1 it will force the program to execute interrupt service routine. Moreover, LVD real-state output can be polled by register PCON1[6]. The following is LVD block diagram:


Figure 19 LVD block diagram
The following table is LVD voltage select table.

| LVDS[3:0] | Voltage |
| :---: | :---: |
| 0000 | -- |
| 0001 | -- |
| 0010 | 2.2 V |
| 0011 | 2.4 V |
| 0100 | 2.6 V |
| 0101 | 2.8 V |
| 0110 | 2.9 V |
| 0111 | 3.0 V |
| 1000 | 3.15 V |
| 1001 | 3.30 V |
| 1010 | 3.45 V |
| 1011 | 3.60 V |
| 1100 | 3.75 V |
| 1101 | 3.90 V |


| LVDS[3:0] | Voltage |
| :---: | :---: |
| 1110 | 4.05 V |
| 1111 | 4.15 V |

Table 12 LVD voltage select

Note:
The hysteresis voltage (from low to high) of LVD is about 0.1 V .
In battery charging applications (detected voltage is from low to high),
the LVD voltage select table should be as followed:

| LVDS[3:0] | Voltage |
| :---: | :---: |
| 0000 | -- |
| 0001 | -- |
| 0010 | $(2.2+0.1) \mathrm{V}$ |
| 0011 | $(2.4+0.1) \mathrm{V}$ |
| 0100 | $(2.6+0.1) \mathrm{V}$ |
| 0101 | $(2.8+0.1) \mathrm{V}$ |
| 0110 | $(2.9+0.1) \mathrm{V}$ |
| 0111 | $(3.0+0.1) \mathrm{V}$ |
| 1000 | $(3.15+0.1) \mathrm{V}$ |
| 1001 | $(3.30+0.1) \mathrm{V}$ |
| 1010 | $(3.45+0.1) \mathrm{V}$ |
| 1011 | $(3.60+0.1) \mathrm{V}$ |
| 1100 | $(3.75+0.1) \mathrm{V}$ |
| 1101 | $(3.90+0.1) \mathrm{V}$ |
| 1110 | $(4.05+0.1) \mathrm{V}$ |
| 1111 | $(4.15+0.1) \mathrm{V}$ |

The LVD control flow is as the following:
Step1: $\quad$ Select LVD voltage by LVDS[3:0]
Step2: $\quad$ Set $C M P C R=0 \times 0 A$
Step3: Set PCON[5]=1 (enable LVD)
Step4: Check LVD status by PCON1[6]
Note: If LVD voltage LVDS[3:0] is changed, user must wait at least 50 us(@F ${ }_{\text {Hоsс }}=1 \mathrm{MHz}$ ) to get correct LVD status by PCON1[6]

### 3.11 Voltage Comparator

NY8A053E provides voltage comparator and internal reference voltage with various analog comparing mode.
The comparator non-inverting and inverting input can share with GPIO.

CMPEN (register PCON[2]) is used to enable and disable comparator. When CMPEN=0(default), comparator is disabled. When CMPEN $=1$, the comparator is enabled. In halt mode the comparator is disabled automatically. The structure of comparator is shown in the following figure:


Figure 20 Comparator block diagram

### 3.11.1 Comparator Reference Voltage (Vref)

The internal reference voltage Vref is built by series resistance to provide different level of reference voltage. RBIAS_H and RBIAS_L are used to select the maximum and minimum values of Vref, and LVDS[3:0] are used to select one of 16 voltage levels.


Figure 21 Vref hardware connection
The Vref is determined by RBIAS_H, RBIAS_L and LVDS[3:0]. The LVDS[3:0] is used to select one out of 16 reference voltages, the table shown below.

| LVDS[3:0] | RBIAS_H=1 <br> RBIAS_L=0 | RBIAS_H=0 <br> RBIAS_L=1 |
| :---: | :---: | :---: |
| 0000 | $67 / 128 V_{D D}$ | $34 / 128 V_{D D}$ |
| 0001 | $64 / 128 V_{D D}$ | $32 / 128 V_{D D}$ |
| 0010 | $59 / 128 V_{D D}$ | $28 / 128 V_{D D}$ |
| 0011 | $54 / 128 V_{D D}$ | $25 / 128 V_{D D}$ |
| 0100 | $50 / 128 \mathrm{~V}_{\mathrm{DD}}$ | $22 / 128 \mathrm{~V}_{\mathrm{DD}}$ |
| 0101 | $47 / 128 \mathrm{~V}_{\mathrm{DD}}$ | $20 / 128 \mathrm{~V}_{\mathrm{DD}}$ |
| 0110 | $45 / 128 \mathrm{~V}_{\mathrm{DD}}$ | $19 / 128 \mathrm{~V}_{\mathrm{DD}}$ |
| 0111 | $44 / 128 \mathrm{~V}_{\mathrm{DD}}$ | $17 / 128 \mathrm{~V}_{\mathrm{DD}}$ |
| 1000 | $42 / 128 \mathrm{~V}_{\mathrm{DD}}$ | $16 / 128 \mathrm{~V}_{\mathrm{DD}}$ |
| 1001 | $40 / 128 \mathrm{~V}_{\mathrm{DD}}$ | $15 / 128 \mathrm{~V}_{\mathrm{DD}}$ |
| 1010 | $38 / 128 \mathrm{~V}_{\mathrm{DD}}$ | $14 / 128 \mathrm{~V}_{\mathrm{DD}}$ |
| 1011 | $37 / 128 \mathrm{~V}_{\mathrm{DD}}$ | $13 / 128 \mathrm{~V}_{\mathrm{DD}}$ |
| 1100 | $35 / 128 \mathrm{~V}_{\mathrm{DD}}$ | $12 / 128 \mathrm{~V}_{\mathrm{DD}}$ |
| 1101 | $34 / 128 \mathrm{~V}_{\mathrm{DD}}$ | $11 / 128 \mathrm{~V}_{\mathrm{DD}}$ |
| 1110 | $33 / 128 \mathrm{~V}_{\mathrm{DD}}$ | $10 / 128 \mathrm{~V}_{\mathrm{DD}}$ |
| 1111 | $32 / 128 \mathrm{~V}_{\mathrm{DD}}$ | $10 / 128 \mathrm{~V}_{\mathrm{DD}}$ |

Table 13 The reference voltage Vref selection table

## Note: The deviation of Vref is $\pm 0.1 \mathrm{~V}$.

Note: RBIAS_L and RBIAS_H MUST be set as "00" before sleep mode or halt mode to prevent current leakage.

The non-inverting input of the comparator is determined by PS[1:0] (register CMPCR[3:2]).
The table is shown below

| PS[1:0] | Non-inverting input |
| :---: | :---: |
| 00 | PA0 |
| 01 | PA2 |
| 10 | Vref |
| 11 | --- |

Table 14 Non-inverting input select
The inverting input of the comparator is determined by $\mathrm{NS}[1: 0]$ (register CMPCR[1:0]).

The table is shown below

| NS[1:0] | Inverting input |
| :---: | :---: |
| 00 | PA1 |
| 01 | PA3 |
| 10 | Bandgap (0.65V) |
| 11 | Vref |

Table 15 Inverting input select
There are two ways to get the comparator output result: one is through register polling, the other is through probing output pad.

Comparator output can be polled by LVDOUT (register PCON1[6] ).

To probe comparator output at output pad, set CMPOE (register OSCCR[6]) to 1, then PB1 will be the real-time state of the comparator output. It is noted that when CMPOE=1, the PWM3 function will be disabled if it is enabled.

### 3.12 Watch-Dog Timer (WDT)

There is an on-chip free-running oscillator in NY8A053E which is used by WDT. As this oscillator is independent of other oscillation circuits, WDT may still keep working during Standby mode and Halt mode.

WDT can be enabled or disabled by a configuration word. When WDT is enabled by configuration word, its operation still can be controlled by register bit WDTEN (PCON[7]) during program execution. Moreover, the mechanism after WDT time-out can reset NY8A053E or issue an interrupt request which is determined by another configuration word. At the same time, register bit /TO (STATUS[4]) will be clear to 0 after WDT time-out. The baseline of WDT time-out period can be $3.5 \mathrm{~ms}, 15 \mathrm{~ms}, 60 \mathrm{~ms}$ or 250 ms which is determined by two configuration words. The time-out period can be lengthened if Prescaler0 is assigned to WDT. Prescaler0 will be assigned to WDT by writing 1 to register bit PSOWDT. The dividing rate of Prescaler0 for WDT is determined by register bits PSOSEL[2:0] and depends on WDT time-out mechanism. The dividing rate is from $1: 1$ to $1: 128$ if WDT time-out will reset NY8A053E and dividing rate is from $1: 2$ to $1: 256$ if WDT time-out will interrupt NY8A053E.

When Prescaler0 is assigned to WDT, the execution of instruction CLRWDT will clear WDT, Prescaler0 and set /TO flag to 1 .

If user selects interrupt for WDT time-out mechanism, register bit WDTIF (INTF[6]) will set to 1 after WDT is expired. It may generate an interrupt request if register bit WDTIE (INTE[6]) and GIE both set to 1. WDTIF will not be clear until firmware writes 0 to WDTIF.

### 3.13 Interrupt

NY8A053E provides two kinds of interrupt: one is software interrupt and the other is hardware interrupt. Software interrupt is caused by execution of instruction INT. There are 6 hardware interrupts:

- Timer0 overflow interrupt.
- Timer1 underflow interrupt.
- WDT timeout interrupt.
- PB input change interrupt.
- External interrupt.
- LVD interrupt

GIE is global interrupt enable flag. It has to be 1 to enable hardware interrupt functions. GIE can be set by ENI instruction and clear to 0 by DISI instruction.

After instruction INT is executed, no matter GIE is set or clear, the next instruction will be fetched from address 0x001. At the same time, GIE will be clear to 0 by NY8A053E automatically. This will prevent nested interrupt from happening. The last instruction of interrupt service routine of software interrupt has to be RETIE. Execution of this instruction will set GIE to 1 and return to original execution sequence.

While any of hardware interrupts is occurred, the corresponding bit of Interrupt Flag Register INTF will be set to 1. This bit will not be clear until firmware writes 0 to this bit. Therefore user can obtain information of which event causes hardware interrupt by polling register INTF. Note that only when the corresponding bit of Interrupt Enable register INTE is set to 1 , will the corresponding interrupt flag be read. And if the corresponding bit of Interrupt Enable Register INTE is set to 1 and GIE is also 1, hardware interrupt will occur and next instruction will be fetched from 0x008. At the same time, the register bit GIE will be clear by NY8A053E automatically. If user wants to implement nested interrupt, instruction ENI can be used as the first instruction of interrupt service routine which will set GIE to 1 again and allow other interrupt events to interrupt NY8A053E again. Instruction RETIE has to be the last instruction of interrupt service routine which will set GIE to 1 and return to original execution sequence.

It should be noted that ENI instruction cannot be placed right before RETIE instruction because ENI instruction in interrupt service routine will trigger nested interrupt, but RETIE will clear internal interrupt processing after jump out of ISR, so it is possible for interrupt flag to be falsely cleared.

### 3.13.1 TimerO Overflow Interrupt

Timer0 overflow (from $0 \times 00$ to $0 x F F$ ) will set register bit TOIF. This interrupt request will be serviced if TOIE and GIE are set to 1.

### 3.13.2 Timer1 Underflow Interrupt

Timer1 underflow (from $0 \times F F$ to $0 \times 00$ ) will set register bit T1IF. This interrupt request will be serviced if T 1 IE and GIE are set to 1 .

### 3.13.3 WDT Timeout Interrupt

When WDT is timeout and the configuration word selects WDT timeout will generate interrupt request, it will set register bit WDTIF. This interrupt request will be serviced if WDTIE and GIE are set to 1 .

### 3.13.4 PB Input Change Interrupt

When PBx, $0 \leq x \leq 7$, is configured as input pin and corresponding register bit WUPBx is set to 1 , a level change on these selected I/O pin(s) will set register bit PBIF. This interrupt request will be serviced if PBIE and GIE are set to 1 . Note when PB0 is both set as level change interrupt and external interrupt, the external interrupt enable EIS=1 will disable PB0 level change operation.

### 3.13.5 External Interrupt

According to the configuration of EIS=1 and INTEDG, the selected active edge on I/O pin PB0 will set register bit INTIF and this interrupt request will be served if INTIE and GIE are set to 1 .

### 3.13.6 LVD Interrupt

When Vod level falls below LVD voltage, LVD flag will go from high to low, and set the register bit LVDIF=1. This interrupt request will be serviced if LVDIE and GIE are set to 1 .

### 3.14 Oscillation Configuration

Because NY8A053E is a dual-clock IC, there are high oscillation (Fhosc) and low oscillation (Flosc) that can be selected as system oscillation (Fosc). The oscillators which could be used as Fhosc are internal high RC oscillator (I_HRC), external high crystal oscillator (E_HXT) and external crystal oscillator (E_XT). The oscillators which could be used as FLosc are internal low RC oscillator (I_LRC) and external low crystal oscillator (E_LXT).


Figure 22 Oscillation Configuration of NY8A053E
There are two configuration words to determine which oscillator will be used as Fhosc. When I_HRC is selected as Fhosc, I_HRC output frequency is determined by three configuration words and it can be $1 \mathrm{M}, 2 \mathrm{M}, 4 \mathrm{M}, 8 \mathrm{M}$, 16 M or 20 MHz . Moreover, external crystal oscillator pads PB4 and PB5 can be used as I/O pins. On the other hand, PB4 can be the output pin of instruction clock according to a configuration word's setting. If Fhosc required external crystal whose frequency ranges from 8 MHz to 20 MHz , E_HXT is recommended. If Frosc required external crystal whose frequency ranges from 455 KHz to 6 MHz , E_XT is recommended. When E_HXT or E_XT is adopted, PB4/PB5 cannot be used as I/O pins. They must be used as crystal output pin and input pin. PB4 is crystal output pin (Xout) and PB5 is crystal input pin (Xin).

There is one configuration word to determine which oscillator will be used as FLosc. When I_LRC is selected, its frequency is centered on 32768 Hz . If FLosc required external crystal, E_LXT is selected and only 32768 Hz crystal is allowed. When E_LXT is adopted, PB4/PB5 cannot be used as I/O pins. They must be used as crystal output pin and input pin. PB4 is crystal output pin (Xout) and PB5 is crystal input pin (Xin). The dual-clock combinations of F ноsc and Flosc are listed below:

| No. | FHOSC | FLOSC |
| :---: | :---: | :---: |
| 1 | I_HRC | I_LRC |
| 2 | E_HXT or E_XT | I_LRC |
| 3 | I_HRC | E_LXT |

Table 16 Dual-clock combinations

When E_HXT, E_XT or E_LXT is used as one of oscillations, the crystal or resonator is connected to Xin and Xout to provide oscillation. Moreover, a resistor and two capacitors are recommended to connect as following figure in order to provide reliable oscillation, refer to the specification of crystal or resonator to adopt appropriate $C 1$ or C 2 value. The recommended value of C 1 and C 2 are listed in the table below.

| Oscillation Mode | Crystal Frequency(Hz) | C1, C2 (pF) |
| :--- | :---: | :---: |
| E_HXT | 16 M | $5 \sim 10$ |
|  | 10 M | $5 \sim 30$ |
|  | 8 M | $5 \sim 20$ |
| E_XT | 4 M | $5 \sim 30$ |
|  | 1 M | $5 \sim 30$ |
|  | 455 K | $10 \sim 100$ |
| E_LXT | 32768 | $10 \sim 30$ |

Table 17 Recommended C1 and C2 Value for Different Kinds of Crystal Oscillation
For 20 MHZ resonator in 2 clock CPU cycle mode, An 18 pF C2 capacitor is a must.
Moreover, for precision 32.768 k crystal, it is recommended to set $\mathrm{C} 1=\mathrm{C} 2=20 \mathrm{pF}$ capacitor.


Figure 23 Connection for External Crystal Oscillation

Either Fhosc or Flosc can be selected as system oscillation Fosc according to the value of register bit SELHOSC (OSCCR[0]). When SELHOSC is 1 , Fhosc is selected as Fosc. When SELHOSC is 0 , Flosc is selected as Fosc. Once Fosc is determined, the instruction clock Finst can be Fosc/2 or Fosc/4 according to value of a configuration word.

### 3.15 Operating Mode

NY8A053E provides four kinds of operating mode to tailor all kinds of application and save power consumptions. These operating modes are Normal mode, Slow mode, Standby mode and Halt mode. Normal mode is designated for high-speed operating mode. Slow mode is designated for low-speed mode in order to save power consumption. At Standby mode, NY8A053E will stop almost all operations except Timer0/Timer1/WDT in order to wake-up periodically. At Halt mode, NY8A053E will sleep until external event or WDT trigger IC to wake-up.

The block diagram of four operating modes is described in the following figure.


Figure 24 Four Operating Modes

### 3.15.1 Normal Mode

After any Reset Event is occurred and Reset Process is completed, NY8A053E will begin to execute program under Normal mode or Slow mode. Which mode is selected after Reset Process is determined by the Startup Clock configuration word. If Startup Clock=fast, NY8A053E will enter Normal mode, if Startup Clock=Slow, NY8A053E will enter Slow mode. At Normal mode, Fhosc is selected as system oscillation in order to provide highest performance and its power consumption will be the largest among four operating modes. After power on or any reset trigger is released, NY8A053E will enter Normal mode after reset process is completed.

- Instruction execution is based on Fhosc and all peripheral modules may be active according to corresponding module enable bit.
- The Flosc is still active and running.
- IC can switch to Slow mode by writing 0 to register bit SELHOSC (OSCCR[0]).
- IC can switch to Standby mode or Halt mode by programming register bits OPMD[1:0] (OSCCR[3:2]).
- For real time clock applications, the NY8A053E can run in normal mode, at the same time the low-frequency clock Low Oscillator Frequency connects to timer0 clock. This is made possible by setting LCKTM0 to 1 and corresponding configuration word Timer0 source setting to 1.


### 3.15.2 Slow Mode

NY8A053E will enter Slow mode by writing 0 to register bit SELHOSC. At Slow mode, Flosc is selected as system oscillation in order to save power consumption but still keep IC running. However, Fhosc will not be disabled automatically by NY8A053E. Therefore user can write 0 to register bit STPHOSC (OSCCR[1]) in slow mode to reduce power consumption further. But it is noted that it is forbidden to enter slow mode and stop Fhosc at the same time, one must enter slow mode first, then disable Fhosc, or the program may hang on.

- Instruction execution is based on FLOSC and all peripheral modules may be active according to corresponding module enable bit.
- FHOSC can be disabled by writing 1 to register bit STPHOSC.
- IC can switch to Standby mode or Halt mode by programming register bits OPMD[1:0].
- IC can switch to Normal mode by writing 1 to SELHOSC.


### 3.15.3 Standby Mode

NY8A053E will enter Standby mode by writing 10b to register bits OPMD[1:0]. At Standby mode, however, Fhosc will not be disabled automatically by NY8A053E and user has to enter slow mode and write 1 to register bit STPHOSC in order to stop Fhosc oscillation. Most of NY8A053E peripheral modules are disabled but Timer can be still active if register bit T0EN/T1EN is set to 1 . Therefore NY8A053E can wake-up after Timer0/Timer1 is expired. The expiration period is determined by the register TMR0/TMR1, FInSt and other configurations for Timer0/Timer1.

- Instruction execution is stop and some peripheral modules may be active according to corresponding module enable bit.
- Fhosc can be disabled by writing 1 to register bit STPHOSC.
- The Flosc is still active and running.
- IC can wake-up from Standby mode if any of
(a) Timer0/Timer1 (overflow/underflow) interrupt
(b) WDT timeout interrupt
(c) PB input change interrupt
(d) INT external interrupt is happened.
(e) LVD interrupt.
- After wake-up from Standby mode, IC will return to Normal mode if SELHOSC=1, IC will return to Slow mode if SELHOSC=0.
- It is not recommended to change oscillator mode (normal to slow / slow to normal) and enter standby mode at the same time.


### 3.15.4 Halt Mode

NY8A053E will enter Halt mode by executing instruction SLEEP or writing 01b to register bits OPMD[1:0]. After entering Halt mode, register bit /PD (STATUS[3]) will be clear to 0 , register bit /TO (STATUS[4]) will be set to 1 and WDT will be clear but keep running.

At Halt mode, all of peripheral modules are disabled, instruction execution is stop and NY8A053E can only wake-up by some specific events. Therefore, Halt mode is the most power saving mode provided by NY8A053E.

- Instruction execution is stop and all peripheral modules are disabled.
- Fhosc and Flosc are both disabled automatically.
- IC can wake-up from Halt mode if any of
(a) WDT timeout interrupt
(b) PB input change interrupt
(c) INT or external interrupt is happened.
- After wake-up from Halt mode, IC will return to Normal mode if SELHOSC=1, IC will return to Slow mode if SELHOSC=0.

Note: Users can change STPHOSC and enter Halt mode in the same instruction.

- It is not recommended to change oscillator mode (normal to slow or slow to normal) and enter halt mode at the same time.


### 3.15.5 Wake-up Stable Time

The wake-up stable time of Halt mode is determined by Configuration word: High Oscillator Frequency or Low Oscillator Frequency. If one of E_HXT, E_XT and E_LXT is selected, the wake-up period would be $512^{*}$ Fosc. And if no XT mode are selected, 16*Fosc would be set as wake-up period. On the other hand, there is no need of wake-up stable time for Standby mode because either Fhosc or Ftosc is still running at Standby mode.

Before NY8A053E enter Standby mode or Halt mode, user may execute instruction ENI. At this condition, NY8A053E will branch to address $0 \times 008$ in order to execute interrupt service routine after wake-up. If instruction DISI is executed or 0 is written to register bit GIE before entering Standby mode or Halt mode, the next instruction will be executed after wake-up.

### 3.15.6 Summary of Operating Mode

The summary of four operating modes is described in the following table.

| Mode | Normal | Slow | Standby | Halt |
| :---: | :---: | :---: | :---: | :---: |
| Fhosc | Enabled | STPHOSC | STPHOSC | Disabled |
| FLosc | Enabled | Enabled | Enabled | Disabled |
| Instruction Execution | Executing | Executing | Stop | Stop |
| Timer0/1 | TOEN / T1EN | T0EN / T1EN | T0EN / T1EN | Disabled |
| WDT | Option and <br> WDTEN | Option and <br> WDTEN | Option and <br> WDTEN | Option and <br> WDTEN |
| Other Modules | Module enable bit | Module enable bit | Module enable bit | All disabled |
| Wake-up Source |  |  | - Timer0 overflow <br> - Timer1 underflow <br> - WDT timeout <br> - WDT timeout <br> - PB input change <br> - INT |  |

Table 18 Summary of Operating Modes

### 3.16 Reset Process

NY8A053E will enter Reset State and start Reset Process when one of following Reset Event is occurred:

- Power-On Reset (POR) is occurred when $V_{D D}$ rising is detected.
- Low-Voltage Reset (LVR) is occurred when operating $V_{D D}$ is below pre-defined voltage.
- Pin RSTb is low state.
- WDT timeout reset.

Moreover, value of all registers will be initialized to their initial value or unchanged if its initial value is unknown. The status bits /TO and /PD could be initialized according to which event causes reset. The /TO and /PD value and its associated event is summarized in the table below.

| Event | /TO | IPD |
| :--- | :---: | :---: |
| POR, LVR | 1 | 1 |
| RSTb reset from non-Halt mode | unchanged | unchanged |
| RSTb reset from Halt mode | 1 | 1 |
| WDT reset from non-Halt mode | 0 | 1 |
| WDT reset from Halt mode | 0 | 0 |
| SLEEP executed | 1 | 0 |
| CLRWDT executed | 1 | 1 |

Table 19 Summary of /TO \& /PD Value and its Associated Event
After Reset Event is released, NY8A053E will start Reset Process. It will wait certain amount of period for oscillation stable no matter what kind of oscillator is adopted. This period is called power-up reset time and is determined by two-bit configuration words which can be $140 \mathrm{us}, 4.5 \mathrm{~ms}, 18 \mathrm{~ms}, 72 \mathrm{~ms}$ or 288 ms . After oscillator is stable, NY8A053E will wait further 16 clock cycles of Fosc (oscillator start-up time, OST) and Reset Process is complete.


Figure 25 Block Diagram of On-Chip Reset Circuit
For slow VDD power-up, it is recommended to use RSTb reset, as the following figure.

- It is recommended the R value should be not greater than $40 \mathrm{k} \Omega$.
- The R1 value $=100 \Omega$ to $1 \mathrm{k} \Omega$ will prevent high current, ESD or Electrical overstress flowing into reset pin.
- The diode helps discharge quickly when power down.


Figure 26 Block Diagram of Reset Application

## 4. Instruction Set

NY8A053E provides 55 powerful instructions for all kinds of applications.

| Inst. |  |  | Operation | Cyc. | Flag |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | 1 | 2 |  |  |  |
| Arithmetic Instructions |  |  |  |  |  |
| ANDAR | R | d | dest = ACC \& R | 1 | Z |
| IORAR | R | d | dest $=A C C \mid R$ | 1 | Z |
| XORAR | R | d | dest $=\mathrm{ACC} \oplus \mathrm{R}$ | 1 | Z |
| ANDIA | i |  | ACC = ACC \& i | 1 | Z |
| IORIA | i |  | ACC $=$ ACC ${ }^{\text {i }}$ | 1 | Z |
| XORIA | i |  | ACC $=\mathrm{ACC} \oplus \mathrm{i}$ | 1 | Z |
| RRR | R | d | Rotate right R | 1 | C |
| RLR | R | d | Rotate left R | 1 | C |
| BSR | R | bit | Set bit in R | 1 | - |
| BCR | R | bit | Clear bit in R | 1 | - |
| INCR | R | d | Increase R | 1 | Z |
| DECR | R | d | Decrease R | 1 | Z |
| COMR | R | d | dest $=\sim R$ | 1 | Z |

Conditional Instructions

| BTRSC | $R$ | bit | Test bit in R, skip if clear | 1 or 2 | - |
| :--- | :---: | :---: | :--- | :--- | :---: |
| BTRSS | $R$ | bit | Test bit in R, skip if set | 1 or 2 | - |
| INCRSZ | $R$ | d | Increase R, skip if 0 | 1 or 2 | - |
| DECRSZ | $R$ | d | Decrease R, skip if 0 | 1 or 2 | - |

Data Transfer Instructions

| MOVAR | R |  | Move ACC to R | 1 | - |
| :--- | :---: | :--- | :--- | :---: | :---: |
| MOVR | R | d | Move R | 1 | Z |
| MOVIA | i |  | Move immediate to ACC | 1 | - |
| SWAPR | R | d | Swap halves R | 1 | - |
| IOST | F |  | Load ACC to F-page SFR | 1 | - |
| IOSTR | F |  | Move F-page SFR to ACC | 1 | - |
| SFUN | S |  | Load ACC to S-page SFR | 1 | - |
| SFUNR | S |  | Move S-page SFR to ACC | 1 | - |
| TOMD |  |  | Load ACC to TOMD | 1 | - |
| TOMDR |  |  | Move TOMD to ACC | 1 | - |
| TABLEA |  | Read ROM | 2 | - |  |



Flag

| ADDAR | R | d | dest $=\mathrm{R}+\mathrm{ACC}$ | 1 | Z, DC, C |
| :---: | :---: | :---: | :---: | :---: | :---: |
| SUBAR | R | d | dest $=$ R + ( ACC) | 1 | Z, DC, C |
| ADCAR | R | d | dest $=R+A C C+C$ | 1 | Z, DC, C |
| SBCAR | R | d | dest $=R+(\sim A C C)+C$ | 1 | Z, DC, C |
| ADDIA | i |  | $A C C=i+A C C$ | 1 | Z, DC, C |
| SUBIA | i |  | ACC $=\mathrm{i}+(\sim A C C)$ | 1 | Z, DC, C |
| ADCIA | i |  | $A C C=i+A C C+C$ | 1 | Z, DC, C |
| SBCIA | i |  | ACC $=\mathrm{i}+(\sim A C C)+C$ | 1 | Z, DC, C |
| DAA |  |  | Decimal adjust for ACC | 1 | C |
| CMPAR | R |  | Compare R with ACC | 1 | Z, C |
| CLRA |  |  | Clear ACC | 1 | Z |
| CLRR |  |  | Clear R | 1 | Z |

Other Instructions

| NOP |  | No operation | 1 | - |
| :--- | :--- | :--- | :---: | :---: |
| SLEEP |  | Go into Halt mode | 1 | /TO, /PD |
| CLRWDT |  | Clear Watch-Dog Timer | 1 | /TO, /PD |
| ENI |  | Enable interrupt | 1 | - |
| DISI |  | Disable interrupt | 1 | - |
| INT |  | Software Interrupt | 3 | - |
| RET |  | Return from subroutine | 2 | - |
| RETIE |  | Return from interrupt <br> and enable interrupt | 2 | - |
| RETIA | i | Return, place immediate <br> in ACC | 2 | - |
| CALLA |  | Call subroutine by ACC | 2 | - |
| GOTOA |  | unconditional branch by ACC | 2 | - |
| CALL | adr | Call subroutine | 2 | - |
| GOTO | adr | unconditional branch | 2 | - |
| LCALL | adr | Call subroutine | 2 | - |
| LGOTO | adr | unconditional branch | 2 | - |

Table 20 Instruction Set

ACC: Accumulator.
adr: immediate address.
bit: bit address within an 8-bit register R .
C: Carry/Borrow bit
C=1, carry is occurred for addition instruction or borrow is NOT occurred for subtraction instruction.
C=0, carry is not occurred for addition instruction or borrow IS occurred for subtraction instruction.
d: Destination
If $d$ is " 0 ", the result is stored in the ACC.
If $d$ is " 1 ", the result is stored back in register $R$.
DC: Digital carry flag.
dest: Destination.
F: F-page SFR, F is $0 \times 5 \sim 0 \times F$.
i: 8-bit immediate data.
PC: Program Counter.
PCHBUF: High Byte Buffer of Program Counter.
/PD: Power down flag bit
/PD=1, after power-up or after instruction CLRWDT is executed.
$/ P D=0$, after instruction SLEEP is executed.
Prescaler: Prescaler0 dividing rate.
$R$ : $R$-page $S F R, R$ is $0 \times 00 \sim 0 \times 3 F$.
S: S-page SFR, S is $0 \times 0 \sim 0 \times 18$.
TOMD: TOMD register.
TBHP: The high-Byte at target address in ROM.
TBHD: Store the high-Byte data at target address in ROM.
/TO: Time overflow flag bit
/TO=1, after power-up or after instruction CLRWDT or SLEEP is executed.
/TO=0, WDT timeout is occurred.
WDT: Watchdog Timer Counter.
Z: Zero flag.

| ADCAR | Add ACC and R with Carry | ADDAR | Add ACC and R |
| :---: | :---: | :---: | :---: |
| Syntax: | ADCAR R, d | Syntax: | ADDAR R, d |
| Operand: | $\begin{aligned} & 0 \leq R \leq 63 \\ & d=0,1 . \end{aligned}$ | Operand: | $\begin{aligned} & 0 \leq R \leq 63 \\ & d=0,1 . \end{aligned}$ |
| Operation: | $\mathrm{R}+\mathrm{ACC}+\mathrm{C} \rightarrow$ dest | Operation: | ACC + R $\rightarrow$ dest |
| Status affected: | Z, DC, C | Status affected: | Z, DC, C |
| Description: | Add the contents of ACC and register R with Carry. If d is 0 , the result is stored in ACC. If $d$ is 1 , the result is stored back to $R$. | Description: | Add the contents of ACC and R. If $d$ is 0 , the result is stored in ACC. If $d$ is 1 , the result is stored back to R. |
| Cycle | 1 | Cycle: | 1 |
| Example: | ADCAR R, d before executing instruction: $A C C=0 \times 12, R=0 \times 34, C=1, d=1 \text {, }$ <br> after executing instruction: $\mathrm{R}=0 \times 47, \mathrm{ACC}=0 \times 12, \mathrm{C}=0$ | Example: | ADDAR R, d before executing instruction: $A C C=0 \times 12, R=0 \times 34, C=1, d=1 \text {, }$ <br> after executing instruction: $\mathrm{R}=0 \times 46, \mathrm{ACC}=0 \times 12, \mathrm{C}=0 .$ |
| ADCIA | Add ACC and Immediate with Carry | ADDIA | Add ACC and Immediate |
| Syntax: | ADCIA | Syntax: | ADDIA |
| Operand: | $0 \leq \mathrm{i}<255$ | Operand: | $0 \leq \mathrm{i}<255$ |
| Operation: | ACC +i+C $\rightarrow$ ACC | Operation: | ACC $+\mathrm{i} \rightarrow \mathrm{ACC}$ |
| Status affected: | Z, DC, C | Status affected: | Z, DC, C |
| Description: | Add the contents of ACC and the 8 -bit immediate data i with Carry. The result is placed in ACC. | Description: | Add the contents of ACC with the 8 -bit immediate data i. The result is placed in ACC. |
| Cycle: | 1 | Cycle: | 1 |
| Example: | ADCIA before executing instruction: $\mathrm{ACC}=0 \times 12, \mathrm{i}=0 \times 34, \mathrm{C}=1$, after executing instruction: $A C C=0 \times 47, C=0 \text {. }$ | Example: | ADDIA <br> before executing instruction: $\mathrm{ACC}=0 \times 12, \mathrm{i}=0 \times 34, \mathrm{C}=1 \text {, }$ <br> after executing instruction: $A C C=0 \times 46, C=0,$ |

ANDAR

Syntax:
Operand:

Operation:
Status affected:
Description:

Cycle:
Example:
AND ACC and $R$

ANDAR R, d
$0 \leq R \leq 63$.
$\mathrm{d}=0,1$.
ACC \& $R \rightarrow$ dest
Z

The content of ACC is AND'ed with $R$. If $d$ is 0 , the result is stored in ACC. If $d$ is 1 , the result is stored back to $R$.

## 1

ANDAR R, d before executing instruction: $A C C=0 \times 5 A, R=0 x A F, d=1$. after executing instruction: $R=0 \times 0 A, A C C=0 \times 5 A, Z=0$.

| ANDIA | AND Immediate with ACC |
| :---: | :---: |
| Syntax: | ANDIA |
| Operand: | $0 \leq \mathrm{i}<255$ |
| Operation: | ACC \& ${ } \rightarrow$ ACC |
| Status affected: | Z |
| Description: | The content of ACC register is AND'ed with the 8 -bit immediate data i . The result is placed in ACC. |
| Cycle: | 1 |
| Example: | ANDIA i <br> before executing instruction: $A C C=0 \times 5 A, i=0 \times A F,$ <br> after executing instruction: $\mathrm{ACC}=0 \times 0 \mathrm{~A}, \mathrm{Z}=0$ |


| BCR | Clear Bit in R |
| :---: | :---: |
| Syntax: | BCR R, bit |
| Operand: | $0 \leq R \leq 63$ |
|  | $0 \leq$ bit $\leq 7$ |
| Operation: | $0 \rightarrow \mathrm{R}$ [bit] |
| Status affected: | -- |
| Description: | Clear the bit ${ }^{\text {th }}$ position in R . |
| Cycle: | 1 |
| Example: | BCR R,B2 <br> before executing instruction: $R=0 \times 5 \mathrm{~A}, \mathrm{~B} 2=0 \times 3,$ <br> after executing instruction: $\mathrm{R}=0 \times 52 .$ |


| BSR | Set Bit in R |
| :---: | :---: |
| Syntax: | BSR R, bit |
| Operand: | $\begin{aligned} & 0 \leq R \leq 63 \\ & 0 \leq \text { bit } \leq 7 \end{aligned}$ |
| Operation: | $1 \rightarrow \mathrm{R}[\mathrm{bit}]$ |
| Status affected: | -- |
| Description: | Set the bit ${ }^{\text {th }}$ position in R . |
| Cycle: | 1 |
| Example: | BSR R,B2 <br> before executing instruction: $\mathrm{R}=0 \times 5 \mathrm{~A}, \mathrm{~B} 2=0 \times 2 \text {, }$ <br> after executing instruction: R=0x5E. |


| BTRSC | Test Bit in R and Skip if Clear |
| :---: | :---: |
| Syntax: | BTRSC R, bit |
| Operand: | $0 \leq \mathrm{R} \leq 63$ |
|  | $0 \leq$ bit $\leq 7$ |
| Operation: | Skip next instruction, if $\mathrm{R}[\mathrm{bit}]=0$. |
| Status affected: | -- |
| Description: | If $R[b i t]=0$, the next instruction which is already fetched is discarded and a NOP is executed instead. Therefore it makes this instruction a two-cycle instruction. |
| Cycle: | 1 or 2(skip) |
| Example: | BTRSC R, B2 <br> Instruction1 <br> Instruction2 <br> before executing instruction: $\mathrm{R}=0 \times 5 \mathrm{~A}, \mathrm{~B} 2=0 \times 2 \text {, }$ <br> after executing instruction: because $R[B 2]=0$, instruction1 will not be executed, the program will start execute instruction from instruction2. |


| BTRSS | Test Bit in R and Skip if Set |
| :---: | :---: |
| Syntax: | BTRSS R, bit |
| Operand: | $\begin{aligned} & 0 \leq R \leq 63 \\ & 0 \leq \text { bit } \leq 7 \end{aligned}$ |
| Operation: | Skip next instruction, if $\mathrm{R}[\mathrm{bit}]=1$. |
| Status affected: | -- |
| Description: | If $R[b i t]=1$, the next instruction which is already fetched is discarded and a NOP is executed instead. Therefore it makes this instruction a two-cycle instruction. |
| Cycle: | 1 or 2(skip) |
| Example: | BTRSS R, B2 <br> Instruction2 <br> Instruction3 <br> before executing instruction: $\mathrm{R}=0 \times 5 \mathrm{~A}, \mathrm{~B} 2=0 \times 3 \text {, }$ <br> after executing instruction: because $R[B 2]=1$, instruction2 will not be executed, the program will start execute instruction from instruction3. |


| CALL | Call Subroutine |
| :---: | :---: |
| Syntax: | CALL adr |
| Operand: | $0 \leq$ adr $<255$ |
| Operation: | PC $+1 \rightarrow$ Top of Stack <br> $\{P C H B U F, a d r\} \rightarrow P C$ |
| Status affected: | -- |
| Description: | The return address $(P C+1)$ is pushed onto top of Stack. The 8 -bit immediate address adr is loaded into $\operatorname{PC}[7: 0]$ and PCHBUF[1:0] is loaded into PC[9:8]. |
| Cycle: | 2 |
| Example: | CALL SUB <br> before executing instruction: <br> PC=A0. Stack pointer=1 after executing instruction: <br> PC=address of SUB, Stack[1] = A0+1, Stack pointer=2. |


| CALLA | Call Subroutine |
| :---: | :---: |
| Syntax: | CALLA |
| Operand: | -- |
| Operation: | PC + $1 \square$ Top of Stack <br> $\{T B H P, A C C\} \rightarrow P C$ |
| Status affected: | -- |
| Description: | The return address $(P C+1)$ is pushed onto top of Stack. The contents of TBHP[1:0] is loaded into PC[9:8] and ACC is loaded into $\mathrm{PC}[7: 0]$. |
| Cycle: | 2 |
| Example: | CALLA <br> before executing instruction: <br> TBHP=0x02, <br> ACC $=0 \times 34$. <br> $\mathrm{PC}=\mathrm{A} 0$. Stack pointer=1. <br> after executing instruction: <br> $P C=0 \times 234$, Stack[1]=A0+1, Stack pointer=2 |


| CLRA | Clear ACC |
| :---: | :---: |
| Syntax: | CLRA |
| Operand: | -- |
| Operation: | $\begin{aligned} & 00 \mathrm{~h} \rightarrow \mathrm{ACC} \\ & 1 \rightarrow \mathrm{Z} \end{aligned}$ |
| Status affected: | Z |
| Description: | $A C C$ is clear and $Z$ is set to 1 . |
| Cycle: | 1 |
| Example: | CLRA <br> before executing instruction: $\mathrm{ACC}=0 \times 55, \quad \mathrm{Z}=0 .$ <br> after executing instruction: $A C C=0 \times 00, Z=1 \text {. }$ |


| CLRR | Clear $R$ |
| :--- | :--- |
| Syntax: | CLRR $\quad \mathrm{R}$ |
| Operand: | $0 \leq R \leq 63$ |
| Operation: | $00 \mathrm{~h} \rightarrow \mathrm{R}$ <br> $1 \rightarrow \mathrm{Z}$ |
| Status affected: | Z |
| Description: | The content of R is clear and Z is <br> set to 1. |
| Cycle: | 1 |


| CLRWDT | Clear Watch-Dog Timer |
| :---: | :---: |
| Syntax: | CLRWDT |
| Operand: | -- |
| Operation: | $\begin{aligned} & 00 \mathrm{~h} \rightarrow \text { WDT, } \\ & 00 \mathrm{~h} \rightarrow \text { WDT prescaler } \\ & 1 \rightarrow \text { /TO } \\ & 1 \rightarrow \text { /PD } \end{aligned}$ |
| Status affected: | /TO, /PD |
| Description: | Executing CLRWDT will reset WDT, Prescaler0 if it is assigned to WDT. Moreover, status bits /TO and /PD will be set to 1 . |
| Cycle: | 1 |
| Example: | CLRWDT <br> before executing instruction: /TO=0 <br> after executing instruction: /TO=1 |
| COMR | Complement R |
| Syntax: | COMR R, d |
| Operand: | $\begin{aligned} & 0 \leq R \leq 63 \\ & d=0,1 . \end{aligned}$ |
| Operation: | $\sim \mathrm{R} \rightarrow$ dest |
| Status affected: | Z |
| Description: | The content of R is complemented. If $d$ is 0 , the result is stored in ACC. If $d$ is 1 , the result is stored back to $R$. |
| Cycle: | 1 |
| Example: | COMR , d before executing instruction: $\mathrm{R}=0 \times \mathrm{A} 6, \mathrm{~d}=1, \mathrm{Z}=0 \text {. }$ <br> after executing instruction: $\mathrm{R}=0 \times 59, \mathrm{Z}=0 .$ |


| CMPAR | Compare ACC and R |
| :---: | :---: |
| Syntax: | CMPAR R |
| Operand: | $0 \leq \mathrm{R} \leq 63$ |
| Operation: | $\mathrm{R}-\mathrm{ACC} \rightarrow$ (No restore) |
| Status affected: | Z, C |
| Description: | Compare ACC and $R$ by subtracting ACC from $R$ with 2's complement representation. The content of ACC and $R$ is not changed. |
| Cycle: | 1 |
| Example: | CMPAR R <br> before executing instruction: $\mathrm{R}=0 \times 34, \mathrm{ACC}=12, \mathrm{Z}=0, \mathrm{C}=0 .$ <br> after executing instruction: $\mathrm{R}=0 \times 34, \mathrm{ACC}=12, \mathrm{Z}=0, \mathrm{C}=1 .$ |


| DAA | Convert ACC Data Format from <br> Hexadecimal to Decimal |
| :--- | :--- |
| Syntax: | DAA |
| Operand: | -- |
| Operation: | ACC(hex) $\rightarrow$ ACC(dec) |
| Status affected: | C |
| Description: | Convert ACC data format from <br> hexadecimal to decimal after <br> addition operation and restore <br> result to ACC. DAA instruction <br> must be placed immediately after <br> addition operation if decimal <br> format is required. Please note <br> that interrupt should be disabled |
|  | before addition instruction and <br> enabled after DAA instruction to |
|  | avoid unexpected result. |
|  | 1 |


| DECR | Decrease $R$ |
| :--- | :--- |
| Syntax: | DECR $R, d$ |
| Operand: | $0 \leq R \leq 63$ <br> $d=0,1$. |
| Operation: | $R-1 \rightarrow$ dest |
| Status affected: | $Z$ |
| Description: | Decrease $R$. If $d$ is 0, the result is <br> stored in $A C C$. If $d$ is 1 , the result is <br> stored back to $R$. |
| Cycle: | 1 |
| Example: | DECR $R, d$ <br> before executing instruction: <br> $R=0 \times 01, d=1, Z=0$. <br> after executing instruction: <br> $R=0 \times 00, Z=1$. |
|  |  |

$\left.\begin{array}{ll}\text { DECRSZ } & \text { Decrease R, Skip if } \mathbf{0} \\ \hline \text { Syntax: } & \text { DECRSZ } R, d \\ \text { Operand: } & \begin{array}{l}0 \leq R \leq 63 \\ d=0,1 .\end{array} \\ \text { Operation: } & \begin{array}{l}R-1 \rightarrow \text { dest, } \\ \text { Skip if result }=0\end{array} \\ \text { Status affected: } & -- \\ \text { Description: } & \begin{array}{l}\text { Decrease } R \text { first. If } d \text { is } 0, \text { the } \\ \text { result is stored in ACC. If } d \text { is } 1, \\ \text { the result is stored back to } R .\end{array} \\ & \begin{array}{l}\text { If result is } 0, \text { the next instruction } \\ \text { which is already fetched is }\end{array} \\ \text { discarded and a NOP is executed } \\ \text { instead. Therefore it makes this } \\ \text { instruction a two-cycle instruction. }\end{array}\right\}$

| DISI | Disable Interrupt Globally |
| :--- | :--- |
| Syntax: | DISI |
| Operand: | -- |
| Operation: | Disable Interrupt, $0 \rightarrow$ GIE |
| Status affected: | -- |
| Description: | GIE is clear to 0 in order to disable <br> all interrupt requests. |
| Cycle: | 1 |


| ENI | Enable Interrupt Globally |
| :--- | :--- |
| Syntax: | ENI |
| Operand: | -- |
| Operation: | Enable Interrupt, $1 \rightarrow$ GIE |
| Status affected: | -- |
| Description: | GIE is set to 1 in order to enable all <br> interrupt requests. |
| Cycle: | 1 |


| GOTO | Unconditional Branch |
| :--- | :--- |
| Syntax: | GOTO adr |
| Operand: | $0 \leq$ adr < 511 |
| Operation: | \{PCHBUF, adr\} $\rightarrow$ PC |
| Status affected: | -- |
| Description: | GOTO is an unconditional branch <br> instruction. The 9-bit immediate <br> address adr is loaded into PC[8:0] <br> and PCHBUF[1] is loaded into |
| PC[9]. |  |


| GOTOA | Unconditional Branch |
| :---: | :---: |
| Syntax: | GOTOA |
| Operand: | -- |
| Operation: | $\{\mathrm{TBHP}, \mathrm{ACC}\} \rightarrow \mathrm{PC}$ |
| Status affected: | -- |
| Description: | GOTOA is an unconditional branch instruction. The content of TBHP[1:0] is loaded into PC[9:8] and $A C C$ is loaded into $P C[7: 0]$. |
| Cycle: | 2 |
| Example: | GOTOA <br> before executing instruction: <br> $\mathrm{PC}=\mathrm{A} 0$. <br> TBHP $=0 \times 02$, <br> $\mathrm{ACC}=0 \times 34$. <br> after executing instruction: $\mathrm{PC}=0 \times 234 .$ |

NY8A053E

| INCR | Increase R |
| :---: | :---: |
| Syntax: | INCR R, d |
| Operand: | $\begin{aligned} & 0 \leq R \leq 63 \\ & d=0,1 . \end{aligned}$ |
| Operation: | $\mathrm{R}+1 \rightarrow$ dest. |
| Status affected: | Z |
| Description: | Increase R. If $d$ is 0 , the result is stored in ACC. If $d$ is 1 , the result is stored back to $R$. |
| Cycle: | 1 |
| Example: | INCR R, d before executing instruction: $\mathrm{R}=0 \mathrm{xFF}, \mathrm{~d}=1, \mathrm{Z}=0 .$ <br> after executing instruction: $\mathrm{R}=0 \times 00, \mathrm{Z}=1 .$ |


| INCRSZ | Increase R, Skip if 0 |
| :---: | :---: |
| Syntax: | INCRSZ R, d |
| Operand: | $\begin{aligned} & 0 \leq R \leq 63 \\ & d=0,1 . \end{aligned}$ |
| Operation: | $\begin{aligned} & \mathrm{R}+1 \rightarrow \text { dest, } \\ & \text { Skip if result = }=0 \end{aligned}$ |
| Status affected: | -- |
| Description: | Increase R first. If $d$ is 0 , the result is stored in ACC. If $d$ is 1 , the result is stored back to $R$. <br> If result is 0 , the next instruction which is already fetched is discarded and a NOP is executed instead. Therefore it makes this instruction a two-cycle instruction. |
| Cycle: | 1 or 2(skip) |
| Example: | INCRSZ R, d <br> instruction2, instruction3. <br> before executing instruction: $\mathrm{R}=0 \mathrm{xFF}, \mathrm{~d}=1, \mathrm{Z}=0 .$ <br> after executing instruction: $R=0 \times 00, Z=1$. And the program will skip instruction2 execution because the operation result is zero. |


| IORAR | OR ACC with R |
| :---: | :---: |
| Syntax: | IORAR R, d |
| Operand: | $\begin{aligned} & 0 \leq R \leq 63 \\ & d=0,1 . \end{aligned}$ |
| Operation: | ACC \| $\mathrm{R}^{\text {dest }}$ |
| Status affected: | Z |
| Description: | OR ACC with $R$. If $d$ is 0 , the result is stored in ACC. If $d$ is 1 , the result is stored back to R . |
| Cycle: | 1 |
| Example: | IORAR R, d before executing instruction: $R=0 \times 50, A C C=0 \times A A, d=1, Z=0 .$ <br> after executing instruction: $R=0 \times F A, A C C=0 \times A A, Z=0$ |


| IORIA | OR Immediate with ACC |
| :--- | :--- |
| Syntax: | IORIA i |
| Operand: | $0 \leq \mathrm{i}<255$ |
| Operation: | ACC \| i $\rightarrow$ ACC |
| Status affected: | Z |
| Description: | OR ACC with 8-bit immediate data <br> i. The result is stored in ACC. |
| Cycle: | 1 <br> Example: |
|  | IORIA i <br> before executing instruction: <br> i=0x50, ACC=0xAA, $\mathrm{Z}=0$. |
|  | after executing instruction: <br> ACC=0xFA, $\mathrm{Z}=0$. |


| IOST | Load F-page SFR from ACC |
| :--- | :--- |
| Syntax: | IOST F |
| Operand: | $0 \leq F \leq 15$ |
| Operation: | ACC $\rightarrow$ F-page SFR |
| Status affected: | -- |
| Description: | F-page SFR F is loaded by content |
|  | of ACC. |
| Cycle: | 1 |
| Example: | IOST F |
|  | before executing instruction: |
|  | F=0x55, ACC=0xAA. <br> after executing instruction: <br>  |


| IOSTR | Move F-page SFR to ACC |
| :--- | :--- |
| Syntax: | IOSTR F |
| Operand: | $5 \leq \mathrm{F} \leq 15$ |
| Operation: | F-page SFR $\rightarrow$ ACC |
| Status affected: | -- |
| Description: | Move F-page SFR F to ACC. |
| Cycle: | 1 |
| Example: | IOSTR F <br> before executing instruction: <br> F=0x55, ACC=0xAA. <br> after executing instruction: <br> F=0x55, ACC=0x55. |
|  |  |


| LCALL | Call Subroutine |
| :--- | :--- |
| Syntax: | LCALL adr |
| Operand: | $0 \leq$ adr $\leq 1023$ |
| Operation: | PC $+1 \rightarrow$ Top of Stack, |
|  | adr $\rightarrow$ PC[9:0] |
| Status affected: | -- |
| Description: | The return address (PC + 1) is <br> pushed onto top of Stack. The <br> $10-b i t ~ i m m e d i a t e ~ a d d r e s s ~ a d r ~ i s ~$ |
|  | loaded into PC[9:0]. |
| Cycle: | 2 <br> Example: |
|  | LCALL SUB <br> before executing instruction: <br> PC=A0. Stack level=1 <br> after executing instruction: <br> PC=address of SUB, Stack[1]= <br>  |


| LGOTO | Unconditional Branch |
| :--- | :--- |
| Syntax: | LGOTO adr |
| Operand: | $0 \leq$ adr $\leq 1023$ |
| Operation: | adr $\rightarrow$ PC[9:0]. |
| Status affected: | -- |
| Description: | LGOTO is an unconditional branch <br> instruction. The 10-bit immediate <br> address adr is loaded into PC[9:0]. |
| Cycle: | 2 <br> Example: |
|  | LGOTO Level <br> before executing instruction: <br> PC=AO. |
|  | after executing instruction: <br> PC=address of Level. |
|  |  |


| MOVIA | Move Immediate to ACC |
| :--- | :--- |
| Syntax: | MOVIA $\quad \mathrm{M}$ |
| Operand: | $0 \leq \mathrm{i}<255$ |
| Operation: | $\mathrm{i} \rightarrow$ ACC |
| Status affected: | -- |
| Description: | The content of ACC is loaded with <br> 8 -bit immediate data i. |
| Cycle: | 1 |
| Example: | MOVIA i <br> before executing instruction: <br> i=0x55, ACC=0xAA. <br> after executing instruction: <br> ACC $=0 \times 55$. |
|  |  |


| MOVAR | Move ACC to R |
| :--- | :--- |
| Syntax: | MOVAR $R$ |
| Operand: | $0 \leq R \leq 63$ |
| Operation: | ACC $\rightarrow R$ |
| Status affected: | -- |
| Description: | Move content of ACC to R. |
| Cycle: | 1 |
| Example: | MOVAR $R$ <br> before executing instruction: <br>  |
|  | $R=0 \times 55$, ACC=0xAA. <br> after executing instruction: <br> $R=0 \times A A, ~ A C C=0 x A A . ~$ |


| MOVR | Move R to ACC or $\mathbf{R}$ |
| :---: | :---: |
| Syntax: | MOVR R, d |
| Operand: | $\begin{aligned} & 0 \leq R \leq 63 \\ & d=0,1 . \end{aligned}$ |
| Operation: | $\mathrm{R} \rightarrow$ dest |
| Status affected: | Z |
| Description: | The content of $R$ is move to destination. If $d$ is 0 , destination is ACC. If $d$ is 1 , destination is $R$ and it can be used to check whether $R$ is zero according to status flag Z after execution. |
| Cycle: | 1 |
| Example: | MOVR R, d before executing instruction: $R=0 \times 0, A C C=0 \times A A, Z=0, d=0 .$ <br> after executing instruction: $\mathrm{R}=0 \times 0, \mathrm{ACC}=0 \times 00, \mathrm{Z}=1 .$ |


| NOP | No Operation |
| :--- | :--- |
| Syntax: | NOP |
| Operand: | -- |
| Operation: | No operation. |
| Status affected: | -- |
| Description: | No operation. |
| Cycle: | 1 |
| Example: |  |

$$
\begin{aligned}
& \text { NOP } \\
& \text { before executing instruction: } \\
& \mathrm{PC}=\mathrm{AO} \\
& \text { after executing instruction: } \\
& \mathrm{PC}=\mathrm{A} 0+1
\end{aligned}
$$

| RETIE | Return from Interrupt and Enable Interrupt Globally | RET | Return from Subroutine |
| :---: | :---: | :---: | :---: |
| Syntax: | RETIE | Syntax: | RET |
| Operand: | -- | Operand: | -- |
| Operation: | Top of Stack $\rightarrow$ PC | Operation: | Top of Stack $\rightarrow$ PC |
|  | $1 \rightarrow \mathrm{GIE}$ | Status affected: | -- |
| Status affected: | -- | Description: | PC is loaded from top of Stack as |
| Description: | The PC is loaded from top of Stack | Cycle: | return address. $2$ |
| Cycle: | 2 | Example: | RET before executing instruction: |
| Example: | RETIE <br> before executing instruction: <br> GIE=0, Stack level=2. <br> after executing instruction: |  | Stack level=2. after executing instruction: PC=Stack[2], Stack level=1. |
|  | $\mathrm{GIE}=1, \quad \mathrm{PC}=$ Stack[2], Stack pointer=1. |  |  |


| RLR | Rotate Left R Through Carry |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Syntax: | RLR R, d |  |  |  |  |  |  |
| Operand: | $\begin{aligned} & 0 \leq R \leq 63 \\ & d=0,1 . \end{aligned}$ |  |  |  |  |  |  |
| Operation: | $\begin{aligned} & \mathrm{C} \rightarrow \operatorname{dest}[0], \mathrm{R}[7] \rightarrow \mathrm{C}, \\ & \mathrm{R}[6: 0] \rightarrow \operatorname{dest}[7: 1] \end{aligned}$ |  |  |  |  |  |  |
| C | R |  |  |  |  |  |  |
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |

Status affected: C
Description: The content of $R$ is rotated one bit to the left through flag Carry. If d is 0 , the result is placed in ACC. If $d$ is 1 , the result is stored back to $R$.

Cycle: $\quad 1$
Example: $\quad$ RLR R, d before executing instruction: $\mathrm{R}=0 \times \mathrm{A} 5, \mathrm{~d}=1, \mathrm{C}=0$.
after executing instruction:
$\mathrm{R}=0 \times 4 \mathrm{~A}, \mathrm{C}=1$.

| RRR | Rotate Right R Through Carry |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Syntax: | RRR R, d |  |  |  |  |  |
| Operand: | $\begin{aligned} & 0 \leq R \leq 63 \\ & d=0,1 . \end{aligned}$ |  |  |  |  |  |
| Operation: | $\begin{aligned} & \mathrm{C} \rightarrow \operatorname{dest}[7], \mathrm{R}[7: 1] \rightarrow \operatorname{dest}[6: 0], \\ & \mathrm{R}[0] \rightarrow \mathrm{C} \end{aligned}$ |  |  |  |  |  |
| $\stackrel{\rightharpoonup}{c}$ | R |  |  |  |  |  |
| $\rightarrow$ b7 | $\mathrm{b}^{6}$ b5 | b4 | b3 | b2 | b1 | b0 |

Status affected: C
Description: The content of $R$ is rotated one bit to the right through flag Carry. If $d$ is 0 , the result is placed in ACC. If d is 1 , the result is stored back to R.

Cycle: $\quad 1$
Example: $\quad$ RRR R, d before executing instruction:
$\mathrm{R}=0 \times \mathrm{A} 5, \mathrm{~d}=1, \mathrm{C}=0$.
after executing instruction:
$R=0 \times 52, C=1$.

| SBCAR | Subtract ACC and Carry from $R$ |
| :--- | :--- |
| Syntax: | SBCAR $R, d$ |
| Operand: | $0 \leq R \leq 63$ <br> $d=0,1$. |
| Operation: | $R+(\sim A C C)+C \rightarrow$ dest |
| Status affected: | Z, DC, C |
| Description: | Subtract ACC and Carry from $R$ <br> with 2's complement <br> representation. If d is 0 , the result <br> is placed in ACC. If $d$ is 1, the <br> result is stored back to $R$. |

Cycle: $\quad 1$
Example:

SBCAR R, d
(a) before executing instruction:

$$
R=0 \times 05, \quad A C C=0 \times 06, \quad d=1,
$$ $\mathrm{C}=0$.

after executing instruction: $\mathrm{R}=0 \times \mathrm{FE}, \mathrm{C}=0 .(-2)$
(b) before executing instruction: $R=0 \times 05, \quad A C C=0 \times 06, \quad d=1$, $\mathrm{C}=1$.
after executing instruction: $\mathrm{R}=0 \times \mathrm{FF}, \mathrm{C}=0 .(-1)$
(c) before executing instruction: $R=0 \times 06, \quad A C C=0 \times 05, \quad d=1$, $\mathrm{C}=0$.
after executing instruction:

$$
R=0 \times 00, C=1 .(-0), Z=1 .
$$

(d) before executing instruction: $R=0 \times 06, \quad A C C=0 \times 05, \quad d=1$, $\mathrm{C}=1$.
after executing instruction: $\mathrm{R}=0 \times 1, \mathrm{C}=1 .(+1)$

| SBCIA | Subtract ACC and Carry from Immediate | SFUNR | Move S-page SFR from ACC |
| :---: | :---: | :---: | :---: |
| Syntax: | SBCIA | Syntax: | SFUNR S |
| Operand: | $0 \leq \mathrm{i}<255$ | Operand: | $0 \leq \mathrm{S} \leq 15$ |
| Operation: | $\mathrm{i}+(\sim A C C)+\mathrm{C} \rightarrow$ dest | Operation: | S-page SFR $\rightarrow$ ACC |
| Status affected: | Z, DC, C | Status affected: | -- |
| Description: | Subtract ACC and Carry from 8-bit immediate data i with 2's complement representation. The result is placed in ACC. | Description: | Move S-page SFR S to ACC. |
|  |  | Cycle: | 1 |
|  |  | Example: | SFUNR S <br> before executing instruction: |
| Cycle: | 1 |  | $S=0 \times 55, A C C=0 \times A A$. |
| Example: | SBCIAi <br> (a) before executing instruction: $i=0 \times 05, A C C=0 \times 06, C=0$. after executing instruction: $\mathrm{ACC}=0 \times \mathrm{FE}, \mathrm{C}=0 .(-2)$ |  | after executing instruction: $S=0 \times 55, A C C=0 \times 55 .$ |
|  | (b) before executing instruction: $\mathrm{i}=0 \times 05, \mathrm{ACC}=0 \times 06, \mathrm{C}=1 \text {. }$ <br> after executing instruction: $\mathrm{ACC}=0 \times F F, \mathrm{C}=0 .(-1)$ |  |  |
|  | (c) before executing instruction: $\mathrm{i}=0 \times 06, \mathrm{ACC}=0 \times 05, \mathrm{C}=0 .$ <br> after executing instruction: $A C C=0 \times 00, C=1 .(-0), Z=1$ |  |  |
|  | (d) before executing instruction: $\mathrm{i}=0 \times 06, \mathrm{ACC}=0 \times 05, \mathrm{C}=1 \text {. }$ | SLEEP | Enter Halt Mode |
|  | $\mathrm{ACC}=0 \times 1, \mathrm{C}=1 .(+1)$ | Syntax: | SLEEP |
|  |  | Operand: | -- |
|  |  | Operation: | OOh $\rightarrow$ WDT, |
|  |  |  | 00h $\rightarrow$ WDT prescaler |
|  |  |  | $1 \rightarrow$ /TO |
| SFUN | Load S-page SFR to ACC |  | $0 \rightarrow$ /PD |
| Syntax: | SFUN S | Status affected: | /TO, /PD |
| Operand: | $0 \leq \mathrm{s} \leq 15$ | Description: | WDT and Prescaler0 are clear to |
| Operation: | ACC $\rightarrow$ S-page SFR |  | to 0 . |
| Status affected: | -- |  | IC enter Halt mode. |
| Description: | S-page SFR S is loaded by content | Cycle: | 1 |
|  | of ACC. | Example: | SLEEP |
| Cycle: | 1 |  | before executing instruction: $/ P D=1, / T O=0 .$ |
| Example: | SFUN S before executing instruction: $S=0 \times 55, A C C=0 \times A A .$ <br> after executing instruction: $\mathrm{S}=0 \times \mathrm{AA}, \mathrm{ACC}=0 \times \mathrm{AA} .$ |  | after executing instruction: $/ \mathrm{PD}=0, / \mathrm{TO}=1 .$ |


| SUBAR | Subtract ACC from R |
| :---: | :---: |
| Syntax: | SUBAR R, d |
| Operand: | $\begin{aligned} & 0 \leq R \leq 63 \\ & d=0,1 . \end{aligned}$ |
| Operation: | $\mathrm{R}-\mathrm{ACC} \rightarrow$ dest |
| Status affected: | Z, DC, C |
| Description: | Subtract ACC from $R$ with 2's complement representation. If $d$ is 0 , the result is placed in ACC. If $d$ is 1 , the result is stored back to $R$. |
| Cycle: | 1 |
| Example: | SUBAR R, d |
|  | (a) before executing instruction: $R=0 \times 05, A C C=0 \times 06, d=1 .$ <br> after executing instruction: $\mathrm{R}=0 \mathrm{xFF}, \mathrm{C}=0 .(-1)$ |
|  | (b) before executing instruction: $R=0 \times 06, A C C=0 \times 05, d=1 .$ <br> after executing instruction: $\mathrm{R}=0 \times 01, \mathrm{C}=1 .(+1)$ |


| SUBIA | Subtract ACC from Immediate |
| :---: | :---: |
| Syntax: | SUBIA i |
| Operand: | $0 \leq \mathrm{i}<255$ |
| Operation: | $\mathrm{i}-\mathrm{ACC} \rightarrow$ ACC |
| Status affected: | Z, DC, C |
| Description: | Subtract ACC from 8-bit immediate data i with 2's complement representation. The result is placed in ACC. |
| Cycle: | 1 |
| Example: | SUBIA <br> (a) before executing instruction: $\mathrm{i}=0 \times 05, \mathrm{ACC}=0 \times 06$ <br> after executing instruction: ACC=0xFF, C=0. (-1) <br> (b) before executing instruction: $\mathrm{i}=0 \times 06, \mathrm{ACC}=0 \times 05, \mathrm{~d}=1, .$ <br> after executing instruction: $A C C=0 \times 01, C=1 .(+1)$ |


| SWAPR | Swap High/Low Nibble in R |
| :---: | :---: |
| Syntax: | SWAPR R, d |
| Operand: | $\begin{aligned} & 0 \leq R \leq 63 \\ & d=0,1 . \end{aligned}$ |
| Operation: | $\begin{aligned} & \mathrm{R}[3: 0] \rightarrow \operatorname{dest}[7: 4] . \\ & \mathrm{R}[7: 4] \rightarrow \operatorname{dest}[3: 0] \end{aligned}$ |
| Status affected: | -- |
| Description: | The high nibble and low nibble of $R$ is exchanged. If $d$ is 0 , the result is placed in ACC. If $d$ is 1 , the result is stored back to $R$. |
| Cycle: | 1 |
| Example: | SWAPR R, d before executing instruction: $\mathrm{R}=0 \times \mathrm{A} 5, \mathrm{~d}=1 \text {. }$ <br> after executing instruction: $\mathrm{R}=0 \times 5 \mathrm{~A} \text {. }$ |

TABLEA Read ROM data

| Syntax: | TABLEA |
| :---: | :---: |
| Operand: | -- |
| Operation: | ```ROM data{ TBHP, ACC } [7:0] ACC ROM data{TBHP, ACC} [13:8] TBHD.``` |
| Status affected: | -- |
| Description: | The 8 least significant bits of ROM pointed by \{TBHP[2:0], ACC\} is placed to ACC. <br> The 6 most significant bits of ROM pointed by \{TBHP[2:0], ACC\} is placed to TBHD[5:0]. |
| Cycle: | 2 |
| Example: | TABLEA <br> before executing instruction: $\mathrm{TBHP}=0 \times 02, \mathrm{CC}=0 \times 34 .$ <br> TBHD $=0 \times 01$. <br> ROM data[0x234]=0x35AA. after executing instruction: <br> TBHD $=0 \times 35, \mathrm{ACC}=0 \times \mathrm{AA}$. |

SWAPR

## Swap High/Low Nibble in $\mathbf{R}$

| TOMD | Load ACC to TOMD | XORAR | Exclusive-OR ACC with R |
| :---: | :---: | :---: | :---: |
| Syntax: | TOMD | Syntax: | XORAR R, d |
| Operand: | -- | Operand: | $0 \leq \mathrm{R} \leq 63$ |
| Operation: | ACC $\rightarrow$ TOMD |  | $\mathrm{d}=0,1$. |
| Status affected: | -- | Operation: | ACC $\oplus_{\mathrm{R}} \rightarrow$ dest |
| Description: | The content of TOMD is loaded by ACC. | Status affected: | $Z$ |
| Cycle: | 1 | Description: | Exclusive-OR ACC with $R$. If $d$ is 0 , the result is placed in ACC. If $d$ is |
| Example: | TOMD before executing instruction: TOMD $=0 \times 55, \mathrm{ACC}=0 \times A A$. after executing instruction: TOMD $=0 \times A A$. |  | 1 , the result is stored back to $R$. |
|  |  | Cycle: | 1 |
|  |  | Example: | XORAR R, d before executing instruction: $\mathrm{R}=0 \times \mathrm{A} 5, \mathrm{ACC}=0 \times \mathrm{F} 0, \mathrm{~d}=1 .$ <br> after executing instruction: $\mathrm{R}=0 \times 55 .$ |


| TOMDR | Move TOMD to ACC |
| :--- | :--- |
| Syntax: | TOMDR |
| Operand: | -- |
| Operation: | TOMD $\rightarrow$ ACC |
| Status affected: | -- |
| Description: | Move the content of TOMD to ACC. |
| Cycle: | 1 |
| Example: | TOMDR <br>  <br>  <br>  <br> before executing instruction <br> after executing instruction <br> ACC=0x55. |


| XORIA | Exclusive-OR Immediate with ACC |
| :---: | :---: |
| Syntax: | XORIA |
| Operand: | $0 \leq \mathrm{i}<255$ |
| Operation: | ACC $\oplus_{i} \rightarrow$ ACC |
| Status affected: | Z |
| Description: | Exclusive-OR ACC with 8-bit immediate data i . The result is stored in ACC. |
| Cycle: | 1 |
| Example: | XORIA <br> before executing instruction: i=0xA5, ACC=0xF0. <br> after executing instruction: ACC=0x55. |

## 5. Configuration Words



| Item | Name | Options |  |
| :---: | :---: | :---: | :---: |
| 25 | Buzzer Output Pin | 1. PB. 7 | 2. PB. 2 |
| 26 | Input Schmitt Trigger | 1 Enable | 2. Disable (1/2 VDD) |
| 27 | Input High Voltage ( $\mathrm{V}_{\text {IH }}$ ) | 1. 0.7 VDD | 2. 0.5 VDD |
| 28 | Input Low Voltage (VIL) | 1. 0.3 VDD | 2. 0.2 VDD |

Table 21 Configuration Words

## 6. Electrical Characteristics

### 6.1 Absolute Maximum Rating

| Symbol | Parameter | Rated Value | Unit |
| :---: | :--- | :---: | :---: |
| $V_{D D}-V_{S S}$ | Supply voltage | $-0.5 \sim+6.0$ | V |
| $\mathrm{~V}_{\mathbb{I}}$ | Input voltage | $\mathrm{V}_{S S}-0.3 \mathrm{~V} \sim \mathrm{~V}_{\mathrm{DD}}+0.3$ | V |
| $\mathrm{~T}_{\mathrm{OP}}$ | Operating Temperature | $-40 \sim+85$ | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{T}_{\mathrm{ST}}$ | Storage Temperature | $-40 \sim+125$ | ${ }^{\circ} \mathrm{C}$ |

### 6.2 DC Characteristics

(All refer Finst $_{\text {=F }}$ Fhosc/4, Fhosc $=16 \mathrm{MHz@I}$ _HRC, WDT enabled, ambient temperature $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ unless otherwise specified.)

| Symbol | Parameter | VDD | Min. | Typ. | Max. | Unit | Condition |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Vdo | Operating voltage | -- | 3.3 | -- | 5.5 | V | Finst $=20 \mathrm{MHz}$ @ I_HRC/2 |
|  |  |  | 2.2 |  |  |  | FInst $=20 \mathrm{MHz}$ @ I_HRC/4 |
|  |  |  | 2.7 |  |  |  | $\mathrm{F}_{\text {INst }}=16 \mathrm{MHz}$ @ E_HXT/2 |
|  |  |  | 1.8 |  |  |  | $\mathrm{F}_{\text {INST }}=16 \mathrm{MHz}$ @ E_HXT/4 |
|  |  |  |  |  |  |  | FINST $=8 \mathrm{MHz}$ @ I_HRC/4 \& I_HRC/2 |
|  |  |  |  |  |  |  | $\mathrm{F}_{\text {INST }}=8 \mathrm{MHz}$ @ E_HXT/4 \& E_HXT/2 |
|  |  |  | 1.8 |  |  |  | $\mathrm{F}_{\text {INST }}=4 \mathrm{MHz}$ @ I_HRC/4 \& I_HRC/2 |
|  |  |  |  |  |  |  | Finst $=4 \mathrm{MHz}$ @ E_XT/4 \& E_XT/2 |
|  |  |  | 1.8 |  |  |  | $\mathrm{F}_{\text {INST }}=32 \mathrm{KHz}$ @ I_LRC/4 \& I_LRC/2 |
|  |  |  |  |  |  |  | $\mathrm{F}_{\text {INST }}=32 \mathrm{KHz}$ @ E_LXT/4 \& E_LXT/2 |
| $\mathrm{V}_{1}$ | Input high voltage | 5 V | 4.0 | -- | -- | V | RSTb (0.8VDD) |
|  |  | 3 V | 2.4 | -- | -- |  |  |
|  |  | 5 V | 3.5 | -- | -- | V | All other I/O pins, EX_CKI, INT CMOS ( $0.7 \mathrm{~V}_{\mathrm{DD}}$ ) |
|  |  | 3 V | 2.1 | -- | -- |  |  |
|  |  | 5 V | 2.5 | -- | -- | V | All other I/O pins, EX_CKI TTL ( 0.5 V DD) |
|  |  | 3V | 1.5 | -- | -- |  |  |
| VIL | Input low voltage | 5 V | -- | -- | 1.0 | V | RSTb (0.2VDD) |
|  |  | 3 V | -- | -- | 0.6 |  |  |
|  |  | 5 V | -- | -- | 1.5 | V | All other I/O pins, EX_CKI, INT CMOS ( $0.3 \mathrm{~V}_{\mathrm{DD}}$ ) |
|  |  | 3 V | -- | -- | 0.9 |  |  |
|  |  | 5 V | -- | -- | 1.0 | V | All other I/O pins, EX_CKITTL ( 0.2 V DD $)$ |
|  |  | 3 V | -- | -- | 0.6 |  |  |
| Іон | Output high current | 5 V | -- | -20 | -- | mA | Vон $=4.0 \mathrm{~V}$ |
|  |  | 3 V | -- | -10 | -- |  | Vон $=2.0 \mathrm{~V}$ |
| lot | Output low current | 5 V | -- | 40 | -- | mA | V ol $=1.0 \mathrm{~V}$ |
|  |  | 3 V | -- | 26 | -- |  |  |
| $\mathrm{I} R$ | IR sink current | 5 V | -- | 40 | -- | mA | Normal IR |
|  |  | 3 V | -- | 26 | -- |  |  |

NY8A053E

| Symbol | Parameter | $\mathrm{V}_{\mathrm{DD}}$ | Min. | Typ. | Max. | Unit | Condition |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Iop | Operating current | Normal Mode |  |  |  |  |  |
|  |  | 5 V | -- | 2.7 | -- | mA | Fhosc=20MHz @ I_HRC/2 \& E_HXT/2 |
|  |  | 3 V | -- | 1.3 | -- |  |  |
|  |  | 5 V | -- | 2.1 | -- | mA | Fhosc=20MHz @ I_HRC/4 \& E_HXT/4 |
|  |  | 3 V | -- | 1.0 | -- |  |  |
|  |  | 5 V | -- | 2.4 | -- | mA | Fhosc=16MHz @ I_HRC/2 \& E_HXT/2 |
|  |  | 3 V | -- | 1.1 | -- |  |  |
|  |  | 5 V | -- | 1.9 | -- | mA | Fhosc $=16 \mathrm{MHz}$ @ I_HRC/4 \& E_HXT/4 |
|  |  | 3 V | -- | 0.8 | -- |  |  |
|  |  | 5 V | -- | 1.5 | -- | mA | Fhosc=8MHz @ I_HRC/2 \& E_HXT/2 |
|  |  | 3 V | -- | 0.7 | -- |  |  |
|  |  | 5 V | -- | 1.3 | -- | mA | Fhosc=8MHz @ I_HRC/4 \& E_HXT/4 |
|  |  | 3 V | -- | 0.5 | -- |  |  |
|  |  | 5 V | -- | 1.1 | -- | mA | Fhosc=4MHz @ I_HRC/2 \& E_HXT/2 |
|  |  | 3 V | -- | 0.5 | -- |  |  |
|  |  | 5 V | -- | 0.9 | -- | mA | Fhosc=4MHz @ I_HRC/4 \& E_HXT/4 |
|  |  | 3 V | -- | 0.4 | -- |  |  |
|  |  | 5 V | -- | 0.9 | -- | mA | Fhosc=1MHz @ I_HRC/2 \& E_HXT/2 |
|  |  | 3 V | -- | 0.4 | -- |  |  |
|  |  | 5 V | -- | 0.8 | -- | mA | Frosc=1MHz @ I_HRC/4 \& E_HXT/4 |
|  |  | 3 V | -- | 0.4 | -- |  |  |
|  |  | Slow mode |  |  |  |  |  |
|  |  | 5 V | -- | 6.0 | -- | uA | Fhosc disabled, FLosc=32KHz @ I_LRC/2 |
|  |  | 3 V | -- | 2.7 | -- |  |  |
|  |  | 5 V | -- | 7.0 | -- | uA | Fhosc disabled, Flosc=32KHz @ E_LXT/2. |
|  |  | 3 V | -- | 2.9 | -- |  |  |
|  |  | 5 V | -- | 4.3 | -- | uA | Fhosc disabled, FLosc=32KHz @ I_LRC/4 |
|  |  | 3 V | -- | 1.8 | -- |  |  |
|  |  | 5 V | -- | 5.3 | -- | uA | Fhosc disabled, <br> Flosc=32KHz @ E_LXT/4. |
|  |  | 3 V | -- | 2.0 | -- |  |  |
| Іттв | Standby current | 5 V | -- | 2.7 | -- | uA | Standby mode, Fhosc disabled, FLosc=32KHz @ I_LRC/4 |
|  |  | 3 V | -- | 1.1 | -- |  |  |
| Ihalt | Halt current | 5 V | -- | -- | 0.5 | uA | Halt mode, WDT disabled. |
|  |  | 3 V | -- | -- | 0.2 |  |  |
|  |  | 5 V | -- | -- | 5.0 | uA | Halt mode, WDT enabled. |
|  |  | 3 V | -- | -- | 3.0 |  |  |
| RPH | Pull-High resistor | 5 V | -- | 50 | -- | $\mathrm{k} \Omega$ | Pull-High resistor |
|  |  | 3 V | -- | 100 | -- |  |  |
| RpL | Pull-Low resistor | 5 V | -- | 50 | -- | k $\Omega$ | Pull-Low resistor |
|  |  | 3 V | -- | 100 | -- |  |  |

### 6.3 OSC Characteristics

(Measurement conditions $V_{D D}$ Voltage, $T_{A}$ Temperature are equal to programming conditions.)

| Parameter | Min. | Typ. | Max. | Unit | Condition |
| :---: | :---: | :---: | :---: | :---: | :--- |
| I_HRC deviation by socket |  |  | $\pm 1$ | $\%$ | Socket installed directly on writer. |
| I_HRC deviation by handler |  |  | $\pm 3$ | $\%$ | Handler condition with correct setup. |
| I_LRC deviation by handler |  |  | $\pm 5$ | $\%$ |  |

### 6.4 Comparator / LVD Characteristics

( $\mathrm{V}_{\mathrm{DD}}=5 \mathrm{~V}, \mathrm{~V}_{\mathrm{Ss}}=0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ unless otherwise specified.)

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Condition |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| VIVR | Comparator input voltage range | 0 | -- | VDD-1.5 | V | $\mathrm{F}_{\text {Hosc }}=1 \mathrm{MHz}$ |
| $\mathrm{T}_{\text {eno }}$ | Comparator enable to output valid | -- | 20 | -- | us | FHosc $=1 \mathrm{MHz}$ |
| Ico | Operating current of comparator | -- | 70 | -- | uA | Fhosc $=1 \mathrm{MHz}$, P2V mode |
| ILvD | Operating current of LVD | -- | 85 | -- | uA | $\mathrm{F}_{\text {ноsc }}=1 \mathrm{MHz}$, LVD $=4.3 \mathrm{~V}$ |
| Elvo | LVD voltage error | -- | -- | 3 | \% | $\mathrm{F}_{\text {ноsc }}=1 \mathrm{MHz}, \mathrm{LVD}=4.3 \mathrm{~V}$ |

### 6.5 Characteristic Graph

### 6.5.1 Frequency vs. VDD of I_HRC


6.5.2 Frequency vs. Temperature of I_HRC


### 6.5.3 Frequency vs. VDD of I_LRC



### 6.5.4 Frequency vs. Temperature of I_LRC



### 6.6 Recommended Operating Voltage

Recommended Operating Voltage (Temperature range: $-40^{\circ} \mathrm{C} \sim+85^{\circ} \mathrm{C}$ )

| Frequency | Min. Voltage | Max. Voltage | LVR : default <br> $\left(25{ }^{\circ} \mathrm{C}\right)$ | LVR: <br> Recommended <br> $\left(-40^{\circ} \mathrm{C} \sim+85{ }^{\circ} \mathrm{C}\right)$ |
| :---: | :---: | :---: | :---: | :---: |
| $20 \mathrm{M} / 2 \mathrm{~T}$ | 3.3 V | 5.5 V | 3.6 V | 3.6 V |
| $16 \mathrm{M} / 2 \mathrm{~T}$ | 2.7 V | 5.5 V | 3.0 V | 3.3 V |
| $20 \mathrm{M} / 4 \mathrm{~T}$ | 2.2 V | 5.5 V | 2.4 V | 2.7 V |
| $16 \mathrm{M} / 4 \mathrm{~T}$ | 1.8 V | 5.5 V | 2.0 V | 2.2 V |
| $8 \mathrm{M}(2 \mathrm{~T}$ or 4 T$)$ | 1.8 V | 5.5 V | 2.0 V | 2.2 V |
| $\leqq 6 \mathrm{M}(2 \mathrm{~T}$ or 4 T$)$ | 1.8 V | 5.5 V | 2.0 V | 2.2 V |

### 6.7 LVR vs. Temperature



## 7. Die Pad Diagram



## 8. Package Dimension

### 8.1 8-Pin Plastic SOP (150 mil)



Note: For 8-pin SOP, 100 units per tube.

|  | INCHES |  |  | MILLIMETERS |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | MIN | TYP | MAX | MIN | TYP | MAX |
| A | 0.183 | - | 0.202 | 4.65 | - | 5.13 |
| B | 0.144 | - | 0.163 | 3.66 | - | 4.14 |
| C | 0.068 | - | 0.074 | 1.35 | - | 1.88 |
| D | 0.010 | - | 0.020 | 0.25 | - | 0.51 |
| F | 0.015 | - | 0.035 | 0.38 | - | 0.89 |
| G | 0.050 BSC | 1.27 BSC |  |  |  |  |
| J | 0.007 | - | 0.010 | 0.19 | - | 0.25 |
| K | 0.005 | - | 0.010 | 0.13 | - | 0.25 |
| L | 0.189 | - | 0.205 | 4.80 | - | 5.21 |
| M | - | - | $8^{\circ}$ | - | - | $8^{\circ}$ |
| P | 0.228 | - | 0.244 | 5.79 | - | 6.20 |

### 8.2 14-Pin Plastic SOP (150 mil)

|  |  | INCHES |  |  | MILLIMETERS |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | MIN | TYP | MAX | MIN | TYP | MAX |
|  | A | 0.337 | - | 0.344 | 8.55 | - | 8.75 |
|  | B | 0.144 | - | 0.163 | 3.66 | - | 4.14 |
|  | C | 0.068 | - | 0.074 | 1.73 | - | 1.88 |
|  | D | 0.017 | - | 0.020 | 0.35 | - | 0.51 |
|  | F | 0.016 | - | 0.044 | 0.40 | - | 1.12 |
|  | G | 0.050 BSC |  |  | 1.27 BSC |  |  |
|  | J | - | 0.004 |  | - | 0.10 | - |
|  | K | 0.005 | - | 0.010 | 0.13 | - | 0.25 |
|  | L | 0.189 | - | 0.205 | 4.80 | - | 5.21 |
|  | M | - | - | $8^{\circ}$ | - | - | $8^{\circ}$ |
|  | P | 0.228 | - | 0.244 | 5.80 | - | 6.20 |

### 8.3 14-Pin Plastic DIP ( 300 mil )



Note: For 14-pin Plastic DIP, 25 units per tube.

## 9. Ordering Information

| P/N | Package Type | Pin Count | Package Width | Shipping |
| :---: | :---: | :---: | :---: | :--- |
| NY8A053E | Die | -- | -- | -- |
| NY8A053ES8 | SOP | 8 | 150 mil | Tape \& Reel: 2.5 K pcs per Reel <br> Tube: 100 pcs per Tube |
| NY8A053ES14 | SOP | 14 | 150 mil | Tape \& Reel: 2.5 K pcs per Reel <br> Tube: 50 pcs per Tube |
| NY8A053EP14 | PDIP | 14 | 300 mil | Tube: 25 pcs per Tube |


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