



九齊科技股份有限公司  
Nyquest Technology Co., Ltd.

DATA SHEET

# NY9L Series

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## RAM Mapping LCD Driver

**Version 1.0**

**May 25, 2016**

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## Revision History

<i>Version</i>	<i>Date</i>	<i>Description</i>	<i>Modified Page</i>
1.0	2016/05/25	First release.	-

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## 1. General Description

The NY9L series IC is a RAM mapping LCD driver. NY9L010A is a 128 dots (32x4). NY9L020x is 256 dots (32x8). NY9L070x (48x16) is 768 dots. These are suitable for LCD application with software configured command. The host controller can communicate with NY9L series via 3-wire SPI interface. Low power consumption performance is for all NY9L series.

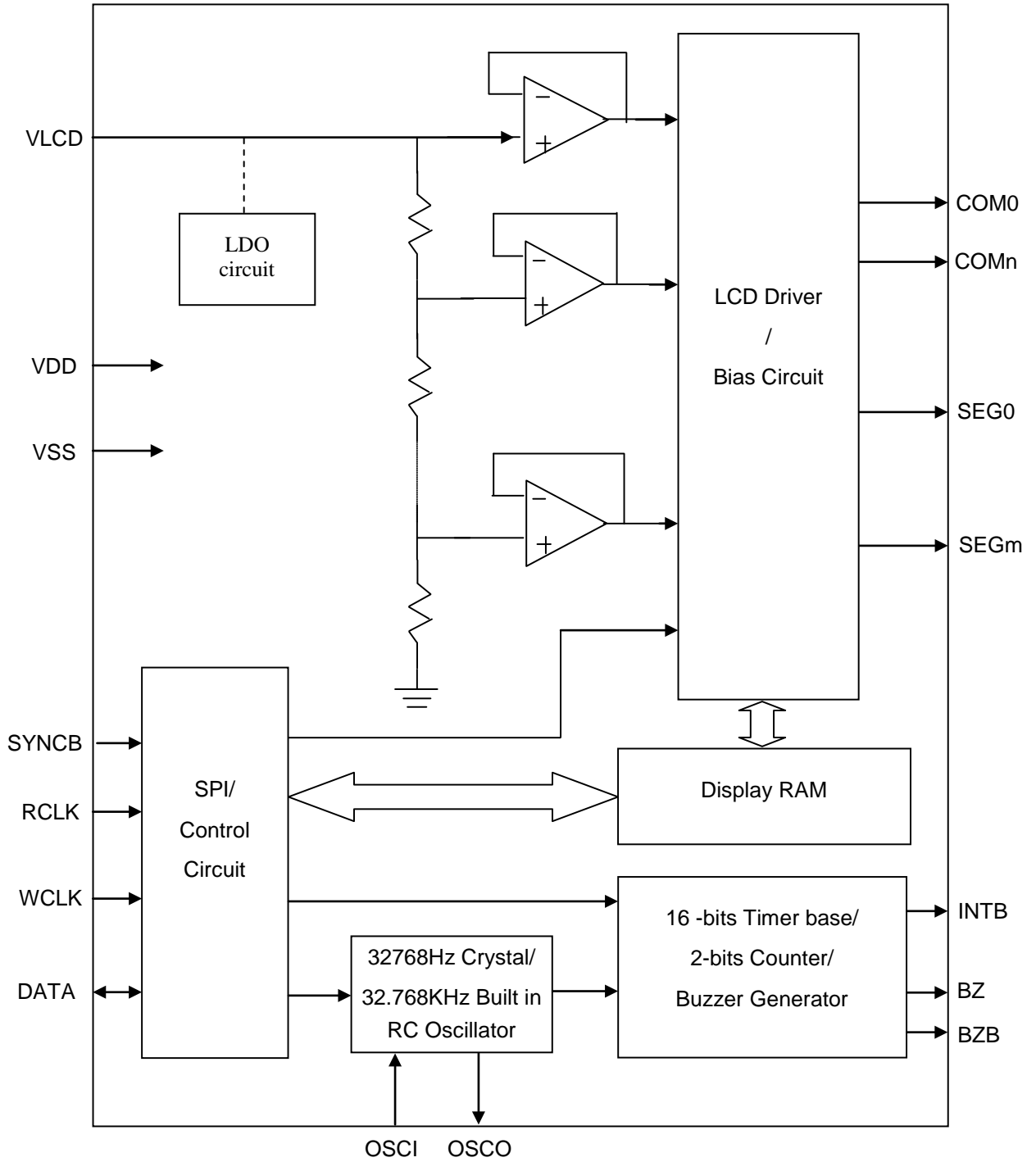
### 1.1 Features

- Operating voltage range: 2.0V to 5.5V. (NY9L070x: 2.0~6.5V)
- System clock: External 256KHz clock input /32.768KHz crystal oscillator/ Built in 32.768KHz RC oscillator with software selection.
- Accurate internal 32.768kHz RC oscillator with +/-3.0% frequency deviation.
- Low operating current. (10uA@3V)
- Low standby current. (<0.1uA)
- Up to 48x16 segment/com (NY9L070x) to support most of LCD panel types.
- Built in 32x4 /32x8 /48x16 bits display RAM.
- Widely LCD application: 1/2 or 1/3 or 1/4 or 1/5 bias. 1/2, 1/3, 1/4, 1/8 or 1/16 duty.
- External LCD power pin for adjusting LCD voltage.
- Internal LCD bias generation with voltage-follower buffers to drive larger LCD panel.
- Built in LDO for LCD power supply.
- 3-wire SPI interface with MCU.
- Provide one 2-bit counter with 8 kinds time base for interrupt request.
- 2KHz/4KHz Buzzer output.
- High 5KV Human Body Mode (HBM) ESD protection.
- Both die and package can be ordered.

### 1.2 Product List

	NY9L010A	NY9L020A	NY9L020B	NY9L020C	NY9L020D	NY9L070A	NY9L070B
<b>COM</b>	4	8	8	8	8	16	16
<b>SEG</b>	32	32	32	32	32	48	48
<b>BIAS</b>	1/2, 1/3	1/4	1/4	1/4	1/4	1/5	1/5
<b>DUTY</b>	1/2, 1/3, 1/4	1/8	1/8	1/8	1/8	1/16	1/16
<b>Built-in OSC</b>	V	V	V	--	--	V	V
<b>Ext. Crystal</b>	V	--	--	V	V	V	V
<b>LDO</b>	--	--	3.0V	--	3.0V	--	4.5V

1.3 Block Diagram



**1.4 Pad Description**

<b>Name</b>	<b>I/O</b>	<b>Description</b>
SYNCB	I	Synchronize pin, low active, with internal pull high resistor 120Kohm@3V.
RCLK	I	SPI Interface pin, Read clock, with internal pull high resistor 120Kohm@3V.
WCLK	I	SPI Interface pin, Write clock, with internal pull high resistor 120Kohm@3V.
DATA	I/O	SPI Interface pin, Bi-direction DATA with internal pull high resistor 120Kohm@3V.
VSS	Power	Ground.
VLCD	Power	LCD power.
VDD	Power	Positive power.
COM0-COMn	O	LCD common pin. (NY9L010A, n=3; NY9L020x, n=7; NY9L070x, n=15)
SEG0-SEGm	O	LCD segment pin (NY9L010A, m=31; NY9L020x, m=31; NY9L070x, m=47)
BZ/ BZB	O	Buzzer frequency output.
INTB	O	Interrupt output, NMOS open drain.
OSCI	I	32768Hz crystal oscillator pin. If the system clock comes from an external clock source, the external clock source should be connected to the OSCI pad. But if an on-chip RC oscillator is selected instead, the both OSCI and OSCO pads can be left open.
OSCO	O	32768Hz crystal oscillator pin.

## 1.5 Electrical Characteristics

### 1.5.1 Absolute Maximum Rating

Symbol	Parameter	Rated Value	Unit
VDD – VSS	Supply voltage	-0.5 ~ +6.0	V
Vin	Input voltage	VSS–0.3V ~ VDD+0.3	V
Top	Operating Temperature	0 ~ +70	°C
Tst	Storage Temperature	-25 ~ +85	°C

### 1.5.2 DC Characteristics

Symbol	Parameter		VDD	Min.	Typ.	Max.	Unit	Condition
VDD	Operating voltage			2.0	3	5.5	V	NY9L010A, NY9L020x
				2.0	3	6.5		NY9L070x
Isb	Halt mode		3			1	uA	Sleep, no load
			5			1		
Iop1	Supply current	Crystal mode	3		10		uA	Crystal Oscillator/ LCD on/ no load
			5		20			
Iop2	Built in RC mode		3		10		uA	Built in RC oscillator/ LCD on/ no load
			5		20			
Iop3	External Clock mode		3		10		uA	External clock/ LCD on/ no load
			5		20			
Iop4	Crystal mode		3		2		uA	Crystal Oscillator/ LCD off/ no load
			5		8			
Iop5	Built in RC mode		3		4.5		uA	Built in RC oscillator/ LCD off/no load
			5		7.5			
Iil	Input current (Internal pull-high)		3		-25		uA	Vii=0V
			5		-83			
Ioh1	Output high current Data		3		-1.0		mA	Voh=2.7V
			5		-3.0			Voh=4.5V
Ioh2	Output high current BZ, BZB		3		-5.0		mA	Voh=2.7V
			5		-10.0			Voh=4.5V
Iol1	Output low current DATA, IRQB		3		2.0		mA	Vol=0.3V
			5		5.5			Vol=0.3V
Iol2	Output low current BZ, BZB		3		8.0		mA	Vol=0.3V
			5		16.0			Vol=0.5V
Icomh	COM output high current		3		-120		uA	Voh=2.7V
			5		-200			Voh=4.5V
Icoml	COM output low current		3		150		uA	Vol=0.3V
			5		250			Vol=0.5V
Isegh	SEG output high current		3		-70		uA	Voh=2.7V
			5		-200			Voh=4.5V
Isegl	SEG output low current		3		120		uA	Vol=0.3V
			5		200			Vol=0.5V



**1.5.3 AC Characteristics**

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
F <sub>SYS1</sub>	System clock		32.768		KHz	Crystal oscillator
F <sub>SYS2</sub>			32.768			Built-in RC oscillator@3V
F <sub>SYS3</sub>			256			External Clock
F <sub>LCD</sub>	LCD frame frequency		128		Hz	1/2 duty
			85.3			1/3 duty
			64			1/4 duty
			64			1/8 duty
			64			1/16 duty
F <sub>RCLK</sub>	Serial interface RCLK pin			150	KHz	@3V, Clock duty 50%
				300		@5V, Clock duty 50%
F <sub>WCLK</sub>	Serial interface WCLK pin			75	KHz	@3V, Clock duty 50%
				150		@5V, Clock duty 50%
T <sub>SYNCB</sub>	Synchronus SYNCB pin		250	75	ns	@3V, High Pulse width

## 2. Instruction

The operation mode of NY9L series is software configuration that instruction format is separated two parts- OPCODE and OPERAND. The OPERAND are ADDRESS, DATA or 9-bits binary code (COMMAND).

### 2.1 Instruction Table

<i>Instruction</i>	<i>OPCODE</i>	<i>OPERAND (x: don't care)</i>	<i>Functional description</i>
READ	110	A5A4A3A2A1A0-D0D1D2D3 (NY9L010A)	Read LCD RAM data A7~A0 is ADDRESS D3~D0 is DATA
		A5A4A3A2A1A0-D0D1D2D3 (NY9L020x)	
		A7A6A5A4A3A2A1A0-D0D1D2D3 (NY9L070x)	
WRITE	101	A5A4A3A2A1A0-D0D1D2D3 (NY9L010A)	Write LCD RAM data A7~A0 is address D3~D0 is data
		A5A4A3A2A1A0-D0D1D2D3 (NY9L020x)	
		A7A6A5A4A3A2A1A0-D0D1D2D3 (NY9L070x)	
SYSDIS	100	0000-0000-x	Disable whole system include oscillator and LCD circuit
OSCEN	100	0000-0001-x	Enable oscillator
LCDDIS	100	0000-0010-x	Disable LCD circuit
LCDEN	100	0000-0011-x	Enable LCD circuit
TBDIS	100	0000-0100-x	Disable Time base
CNTDIS	100	0000-0101-x	Disable Counter
TBEN	100	0000-0110-x	Enable Time base
CNTEN	100	0000-0111-x	Enable Counter
BZDIS	100	0000-1000-x	Disable Buzzer
BZEN	100	0000-1001-x (NY9L010A only)	Enable Buzzer
CLRTB	100	0000-1101-x	Reset Time base
CLRCNT	100	0000-1111-x	Reset Counter
RTC	100	0001-01xx-x	Select 32768Hz Crystal Oscillator
RC32K	100	0001-10xx-x	Select built in RC 32.768KHz
EXTCK	100	0001-11xx-x	Select external 256KHz clock
BIAS2C2	100	0010-00x0-x (NY9L010A only)	1/2 Bias 1/2 duty

<i>Instruction</i>	<i>OPCODE</i>	<i>OPERAND (x: don't care)</i>	<i>Functional description</i>
BIAS2C3	100	0010-01x0-x (NY9L010A only)	1/2 Bias 1/3 duty
BIAS2C4	100	0010-10x0-x (NY9L010A only)	1/2 Bias 1/4 duty
BIAS3C2	100	0010-00x1-x (NY9L010A only)	1/3 Bias 1/2 duty
BIAS3C3	100	0010-01x1-x (NY9L010A only)	1/3 Bias 1/3 duty
BIAS3C4	100	0010-10x1-x (NY9L010A only)	1/3 Bias 1/4 duty
BZ4K	100	010x-xxxx-x	4KHz Buzzer frequency
BZ2K	100	0110-xxxx-x	2KHz Buzzer frequency
INTDIS	100	100x-0xxx-x	Disable INTB output
INTEN	100	100x-1xxx-x	Enable INTB output
TB1HZ	100	101x-0000-x	1Hz Time base frequency
TB2HZ	100	101x-0001-x	2Hz Time base frequency
TB4HZ	100	101x-0010-x	4Hz Time base frequency
TB8HZ	100	101x-0011-x	8Hz Time base frequency
TB16HZ	100	101x-0100-x	16Hz Time base frequency
TB32HZ	100	101x-0101-x	32Hz Time base frequency
TB64HZ	100	101x-0110-x	64Hz Time base frequency
TB128HZ	100	101x-0111-x	128Hz Time base frequency

## 2.2 Clock Option

NY9L provides 3 clocking modules to operate. They are external clock source, RC ring oscillators, and 32768Hz crystal module. The users can select the clock sources based on the application. To utilize the precise timing application, two pins are needed to connect with external crystal module and set RTC instruction. The frequency of external clock source would be 256KHz to generate the suitable time base.

<i>Options</i>	<i>Instruction</i>	<i>Selected Items</i>
	SYSDIS	Disable oscillator
	OSCEN	Enable oscillator
OSC	RTC	32768Hz Crystal oscillator
	RC32K	Built in RC 32.768KHz oscillator
	EXTCK	External 256KHz clock source

The structure of clock source modulation is shown in Fig.1.

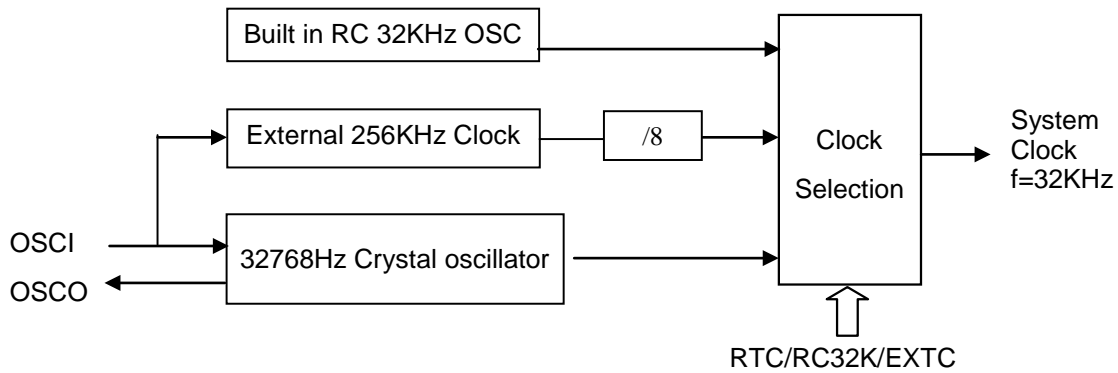


Fig.1: OSC modulation

### 2.3 Interrupt Option

NY9L series have one interrupt output that play two kind roles. One is repeat time toggle and the other is one shot trigger. When it is repeat time toggle, INTB is time base output. Otherwise, INTB is one shot trigger when it is counter output. Interrupt option table should be set below,

Options	Instruction	Selected Items
INT	INTDIS	Disable INTB output
	INTEN	Enable INTB output
	TBDIS	Disable Time base
	TBEN	Enable Time base
	CLRTB	Reset Time base
	CNTDIS	Disable Counter
	CNTEN	Enable Counter
	CLRCNT	Reset Counter
TBkHZ	Time base frequency k=1, 2, 4, 8, 16, 32, 64, 128	

The structure of interrupt source modulation is shown in Fig.2.

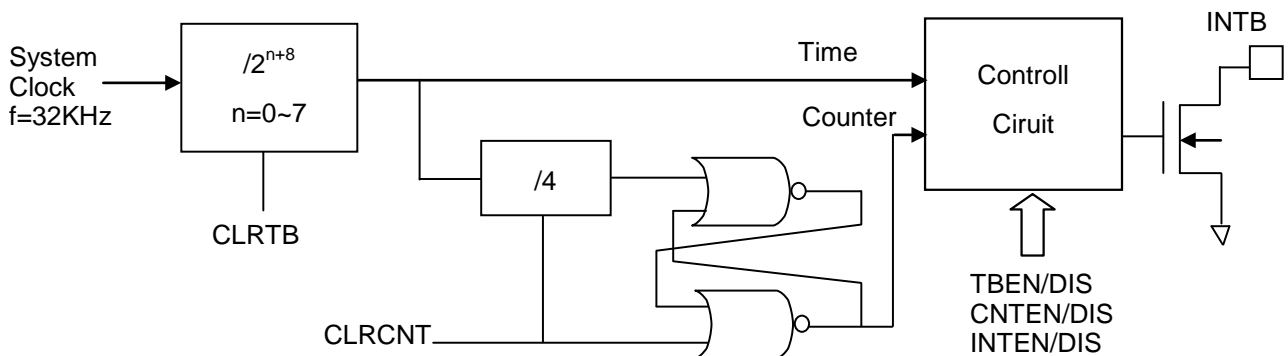


Fig.2: Interrupt source

## 2.4 Buzzer Option

A pair of differential sign, BZ and BZB, can generate a 2KHz or 4KHz tone.

Buzzer option table should be set below.

<i>Options</i>	<i>Instruction</i>	<i>Selected Items</i>
BUZZER	BZDIS	Buzzer disable
	BZEN	Buzzer enable
	BZ4K	4KHz Buzzer frequency
	BZ2K	2KHz Buzzer frequency

NY9L020x and NY9L070x have not BZEN instruction, because those are automatic enable Buzzer output when set BZ2K or BZ4K instruction.

## 2.5 LCD Option

Using properly NY9L series can drive different LCD display panel. Compared with NY9L020x and NY9L070x have one kind of bias and duty, the NY9L010A has different bias and duty setting.

The LCD option should be set below.

<i>Options</i>	<i>Assignment</i>	<i>Selected Items</i>
LCD	LCDDIS	Disable LCD circuit
	LCDEN	Enable LCD circuit
	BIASxCy	1/x Bias, 1/y duty for NY9L010A x=2 or 3; y=2 or 3 or 4;

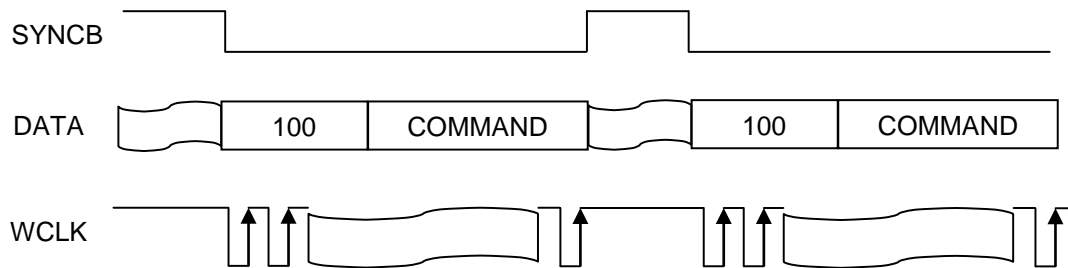
### 3. System Control

The host controller communicate NY9L series with the 3-wire SPI interface. It must keep SYNCB logic low level when send instruction through the serial interface. If SYNCB is logic high, NY9L will ignore any data on the serial interface. The data must transfer form the MSB of each instruction. The NY9L latches the data at each WCLK rising edge. The other hand, the host controller could latch RAM data at RCLK rising edge because that the NY9L series clocks out RAM data at RCLK falling edge .

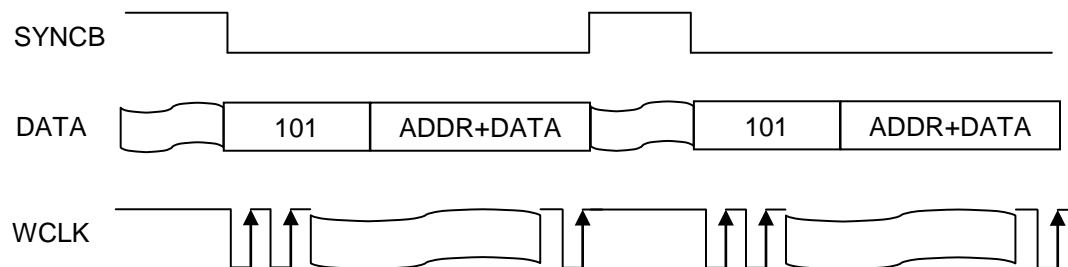
#### 3.1 Standard Procedure

For NY9L series, the standard instruction procedure needs OPCODE and OPERAND.

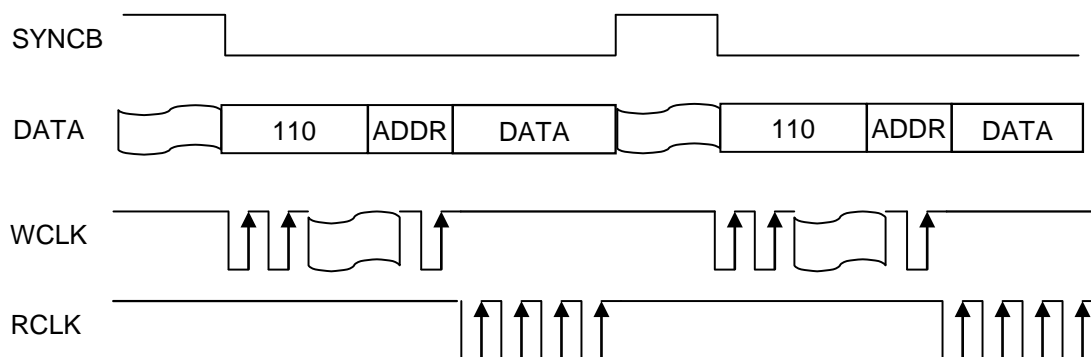
**(I) OPCODE=100**



**(II) OPCODE=101 (WRITE)**



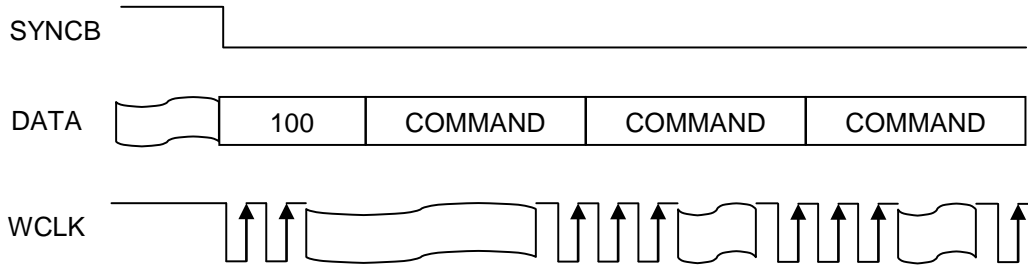
**(III) OPCODE=110 (READ)**



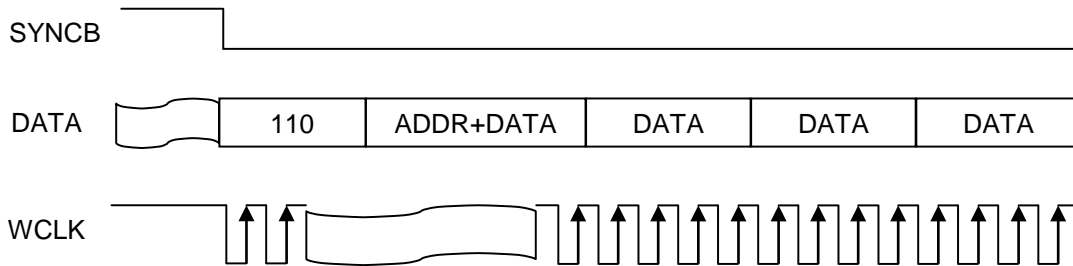
**3.2 Successive Mode**

In the successive instruction mode, the procedure can omit the OPCODE when that is the same as before. If the instruction is WRITE or READ, NY9L will also increase address automatically before next OPERAND. Therefore, the next OPERAND are DATA only without ADDRESS in the successive instruction mode.

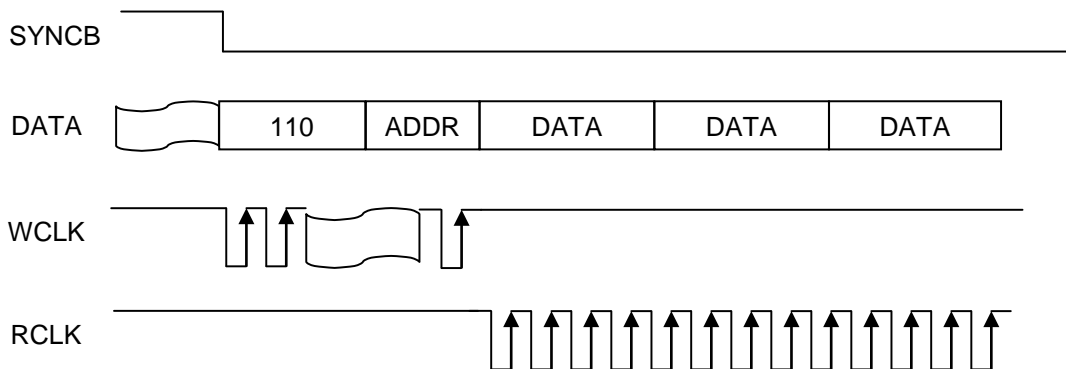
**(I) OPCODE=100**



**(II) OPCODE=101 (WRITE)**



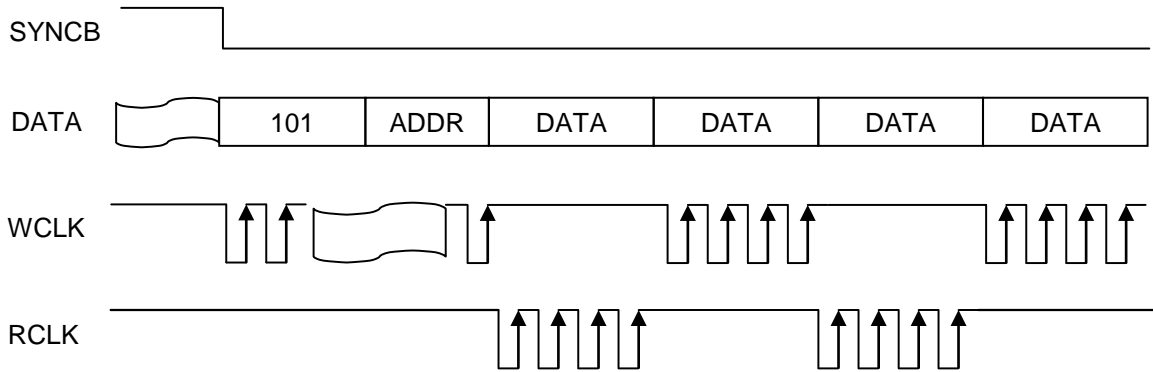
**(III) OPCODE=110 (READ)**



### 3.3 Read-Modify-Write

If the instruction is WRITE, the host controller drives RCLK after WCLK at finishing ADDRESS in the OPERAND, then the system acts as the READ-after-WRITE mode.

**OPCODE=101 (WRITE)**



### 3.4 Serial Sequence

The COMMAND, ADDR and DATA serial sequence is as below:

COMMAND: C8~C0

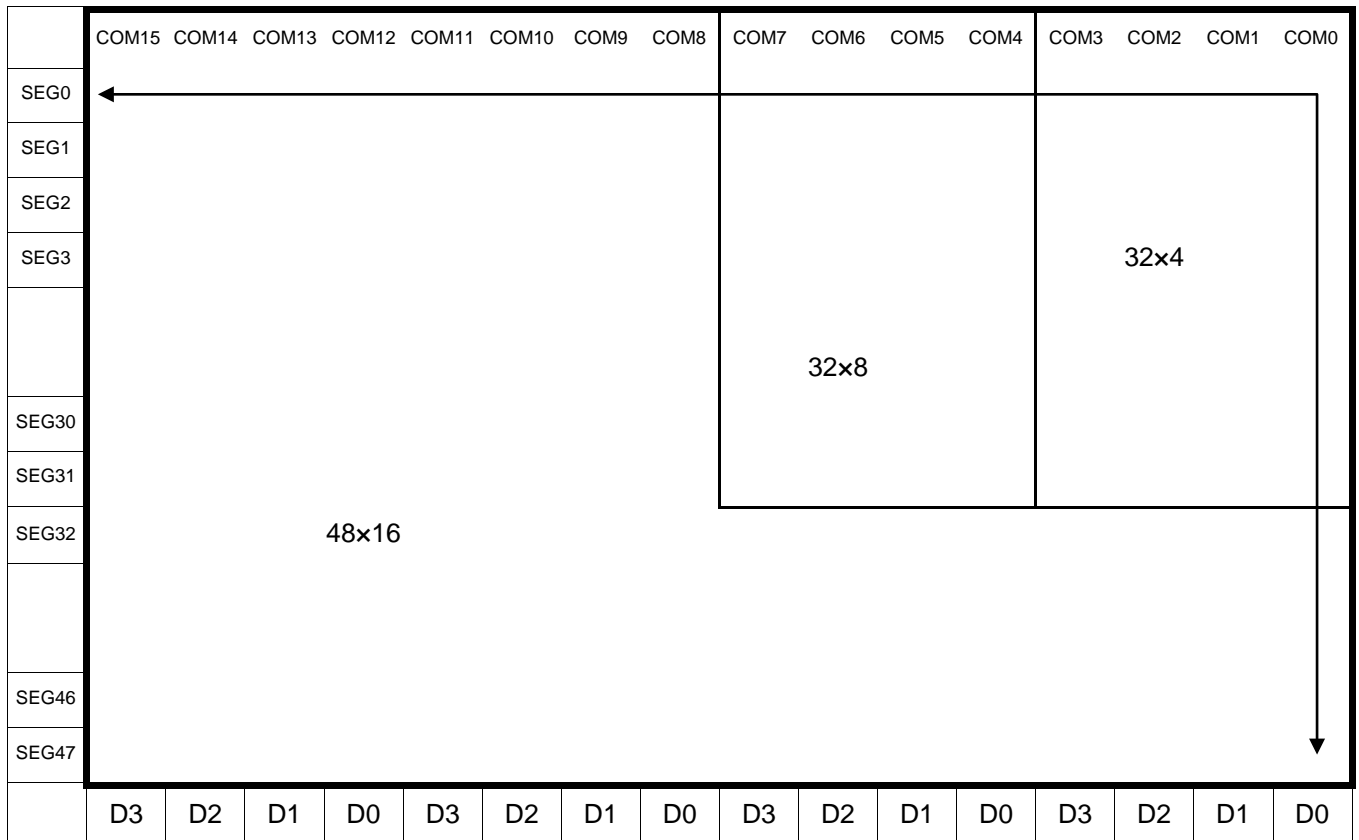
ADDR: An~A0, n: 5 or 7

DATA: D0~D3



### 4. RAM Organization

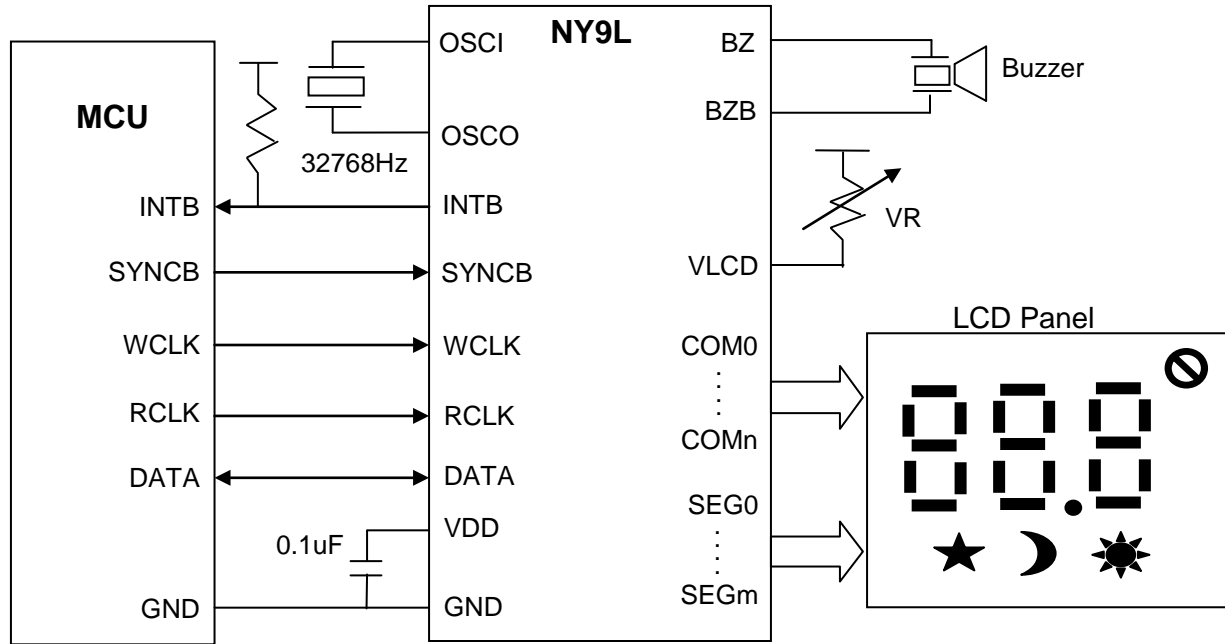
NY9L series provides the users to drive LCD panel specified up to 16 common pin x 48 segment pins to match the most common-used panels. There are maximum 768 pixel for LCD display (NY9L070x). The RAM map is organized into 32x4 bits (NY9L010A), 32x8 bits(NY9L020x), and 48x16 bits(NY9L070x). The first RAM bit is correspond to the SEG0 with respect to COM0.



ADDR	NY9L010A					NY9L020x					NY9L070x				
	SEG	D0	D1	D2	D3	SEG	D0	D1	D2	D3	SEG	D0	D1	D2	D3
0	0	COM0	COM1	COM2	COM3	0	COM0	COM1	COM2	COM3	0	COM0	COM1	COM2	COM3
1	1	COM0	COM1	COM2	COM3	0	COM4	COM5	COM6	COM7	0	COM4	COM5	COM6	COM7
2	2	COM0	COM1	COM2	COM3	1	COM0	COM1	COM2	COM3	0	COM8	COM9	COM10	COM11
3	3	COM0	COM1	COM2	COM3	1	COM4	COM5	COM6	COM7	0	COM12	COM13	COM14	COM15
4	4	COM0	COM1	COM2	COM3	2	COM0	COM1	COM2	COM3	1	COM0	COM1	COM2	COM3
5	5	COM0	COM1	COM2	COM3	2	COM4	COM5	COM6	COM7	1	COM4	COM5	COM6	COM7
....	....					....					....				

### 5. LCD Control

This chapter is mainly to state the power supply for LCD and how it displays on the panel with the corresponding setting. The typical application is shown in Fig.3.



$$VLCD = VDD * R_{built-in} / (R_{built-in} + VR)$$

**Note:  $R_{built-in}$  is 1.75M Ohms**

Fig.3: Application circuit

#### 5.1 LCD Power Supply

NY9L series provides the built-in cascade resistance to divide voltage source (VLCD) for satisfying the different bias settings. For NY9L010A, it contains 1/2, 1/3 bias settings for user's LCD panels. For NY9L020x and NY9L070x, they are 1/4, 1/5 bias separately. The user can also utilize external resistors to adjust the LCD power. For example when VDD works at 5V, user must adjust  $VR = 420k\Omega \pm 20\%$  to fit LCD display  $VLCD = 4V$ . The following lists voltage level of corresponding bias settings.

Bias	Voltage Level
1/2	GND, VLCD/2, VLCD
1/3	GND, VLCD/3, 2*VLCD/3, VLCD
1/4	GND, VLCD/4, 2*VLCD/4, 3*VLCD/4, VLCD
1/5	GND, VLCD/5, 2*VLCD/5, 3*VLCD/5, 4*VLCD/5, VLCD

NY9L020B, NY9L020D and NY9L070B have built-in LDO to supply LCD power. Users don't need to connect external power for VLCD.

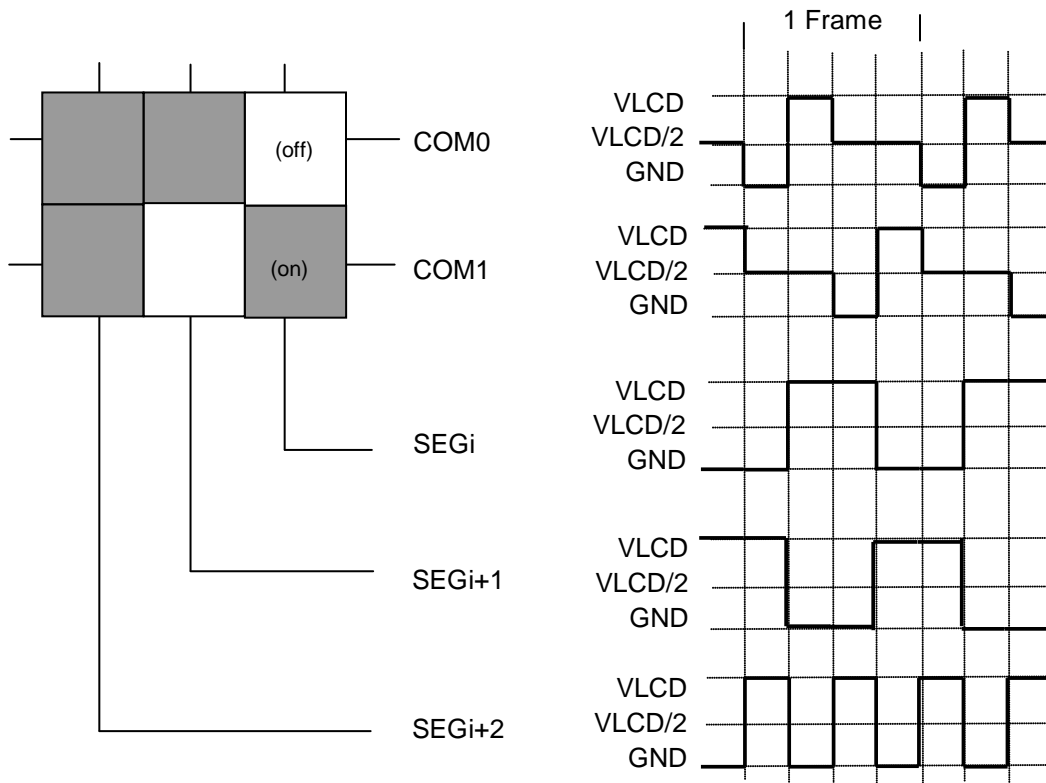
Type	NY9L020B & NY9L020D	NY9L070B
LDO voltage	3V	4.5V

**5.2 LCD Display System**

For the variety of panels, each display system should be different segment and common combination. NY9L010A support 1/2, 1/3 or 1/4 duty and maximum 32 segments. NY9L020x is 1/8 duty and maximum 32 segments. NY9L070x works as 1/16 duty and maximum 48 segments. Logic “0” in the RAM bit-map indicate the “off” state of the LCD segment; Logic “1” indicate “on” state. Here list several LCD waveform of NY9L series.

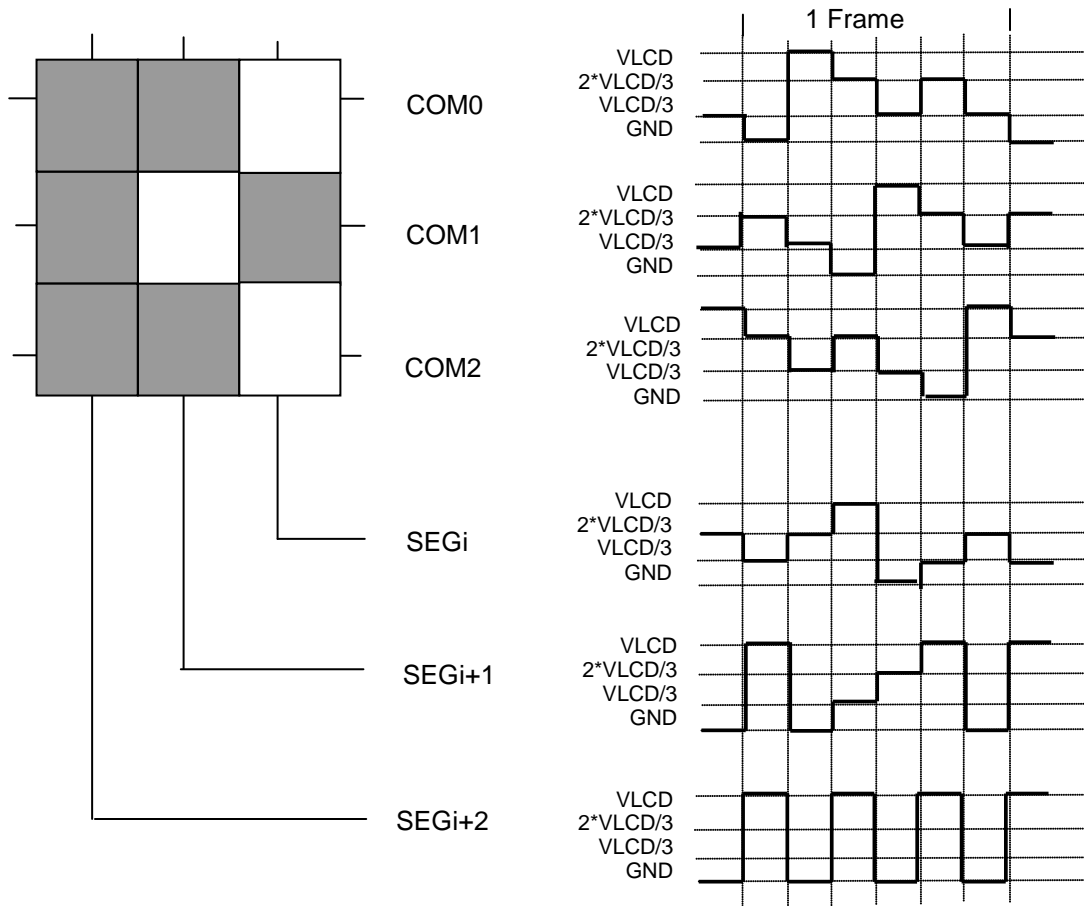
(I) 1/2 duty and 1/2 bias (NY9L010A)

Frame rate= 128Hz



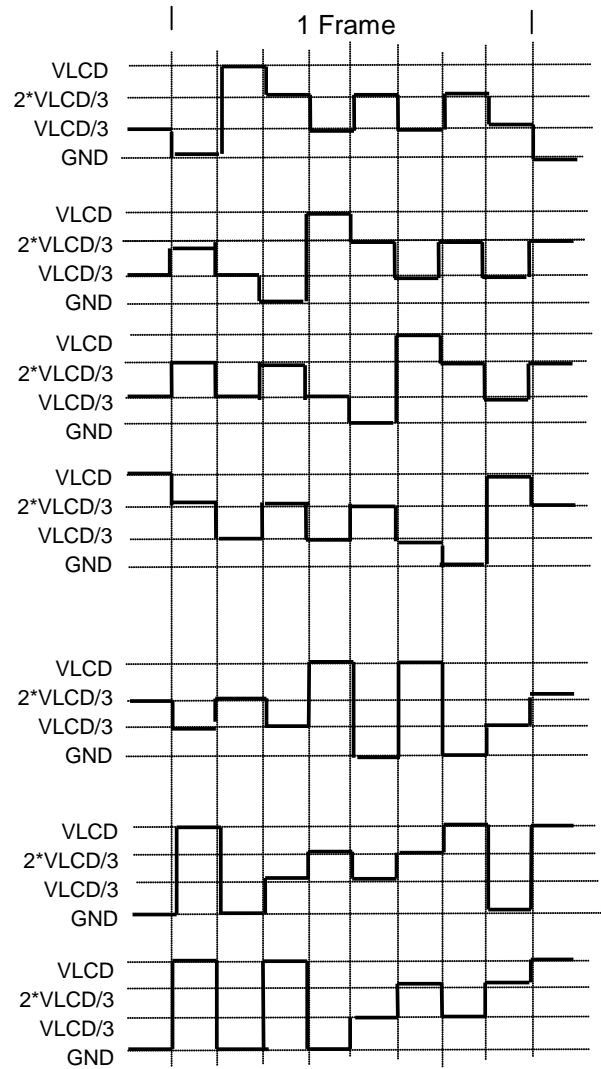
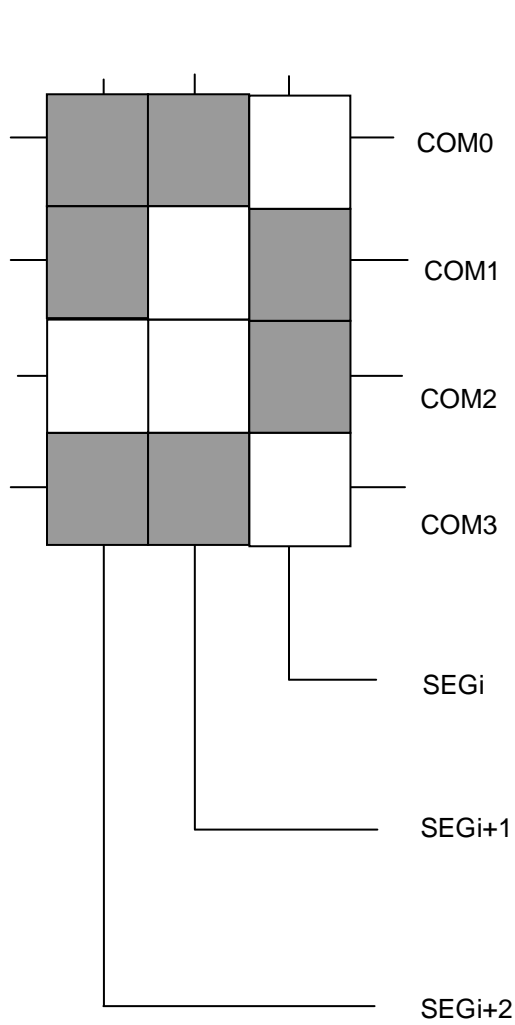
(II) 1/3 duty and 1/3 bias (NY9L010A)

Frame rate = 85.3Hz



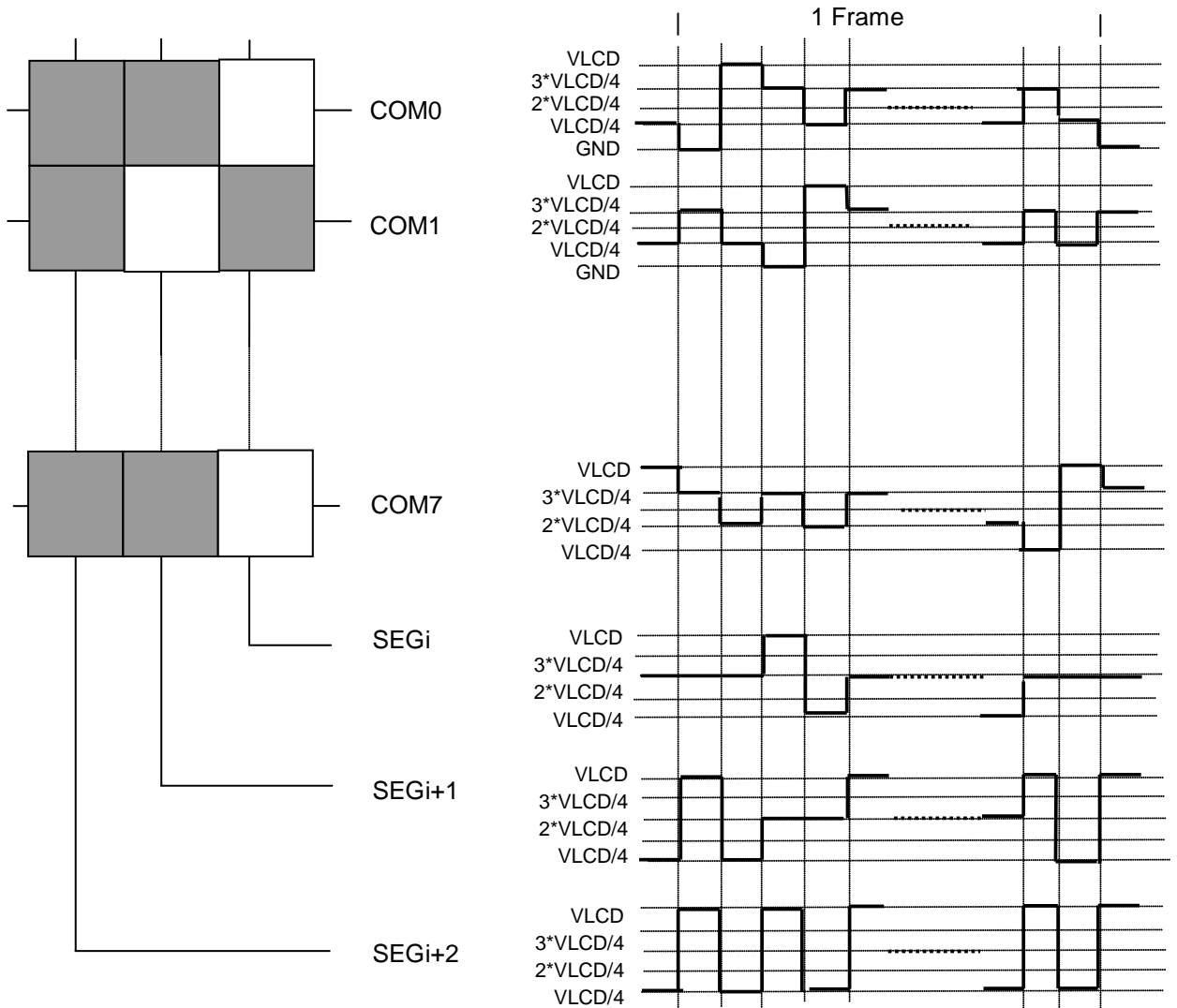
(III) 1/4 duty and 1/3 bias (NY9L010A)

Frame rate=64Hz



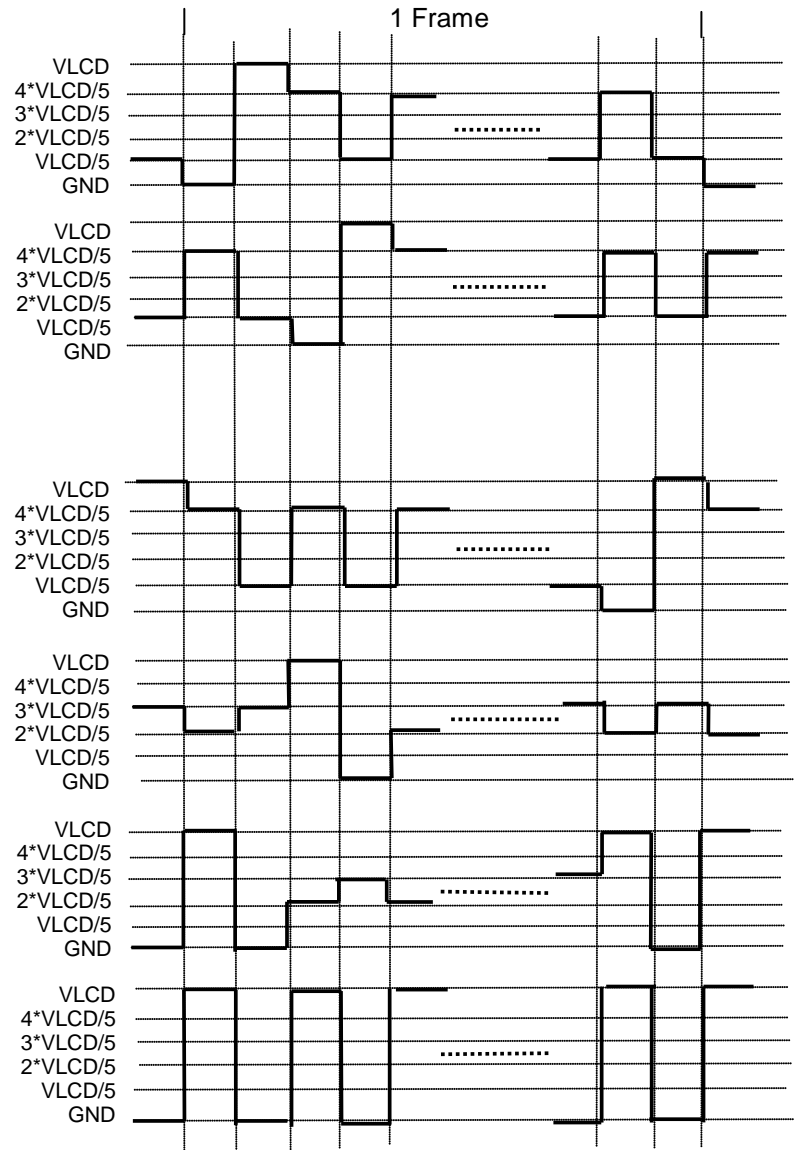
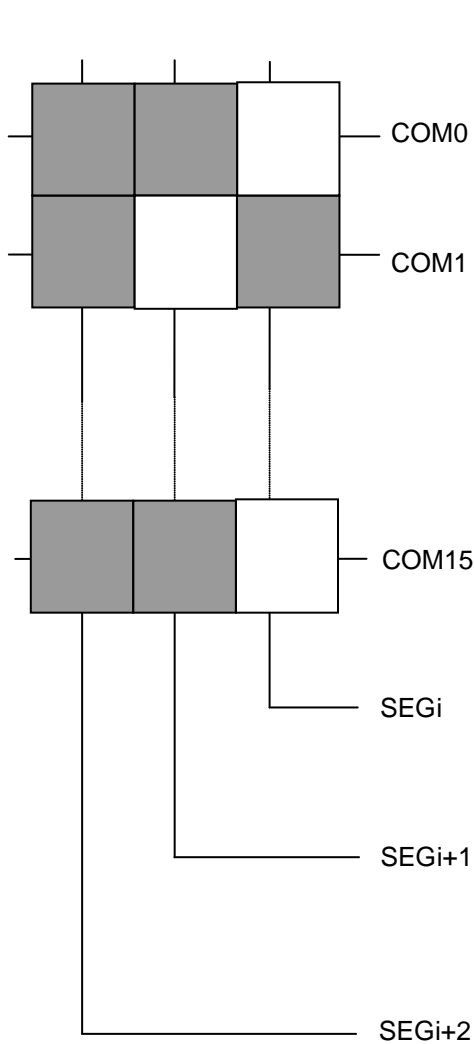
(IV) 1/8 duty and 1/4 bias (NY9L020x)

Frame rate =64Hz



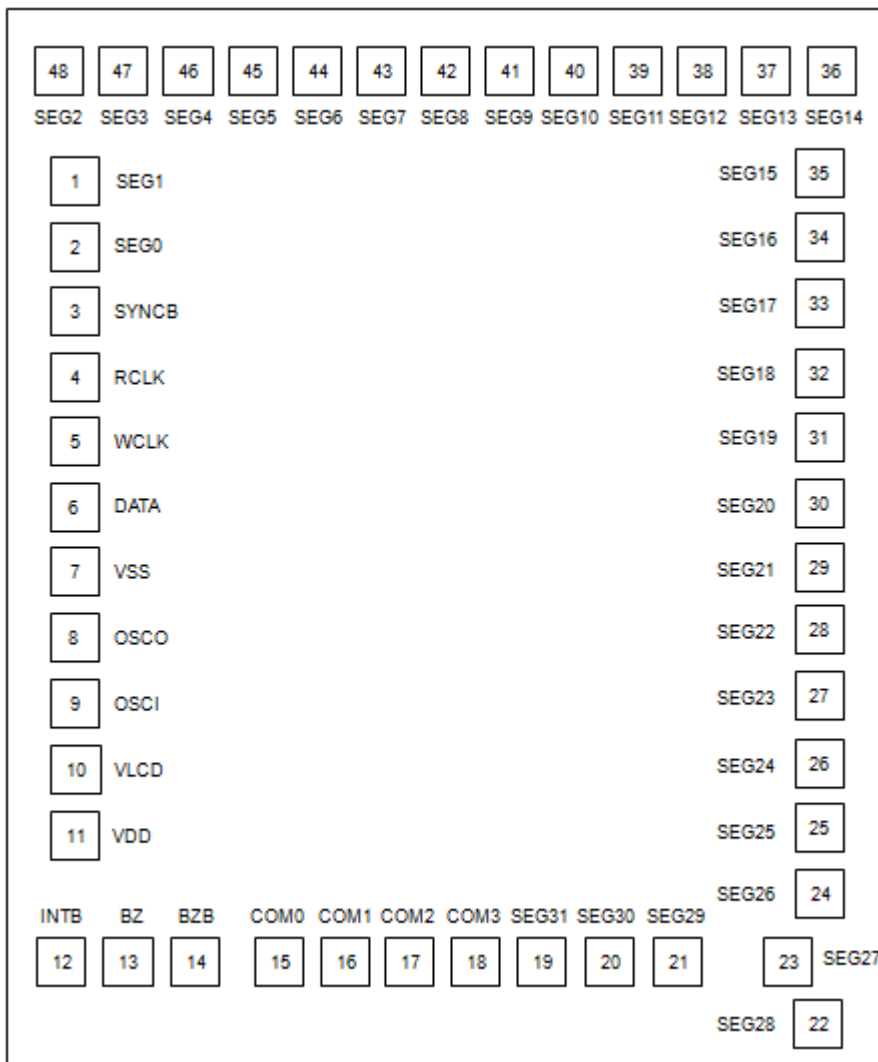
(V) 1/16 duty 1/5 bias (NY9L070x)

Frame rate =64Hz



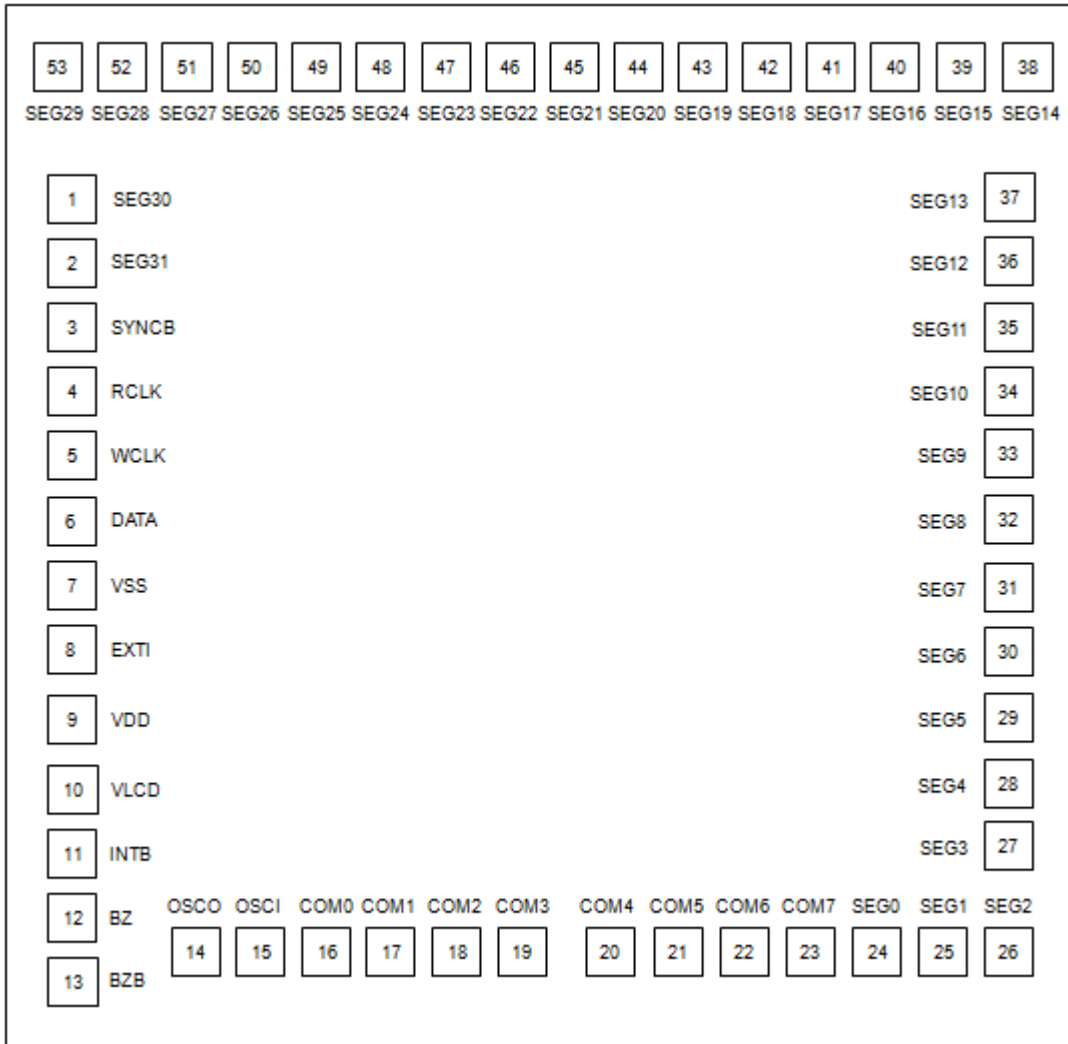
## 6. Die Pad Diagram

### 6.1 NY9L010A





**6.2 NY9L020x**



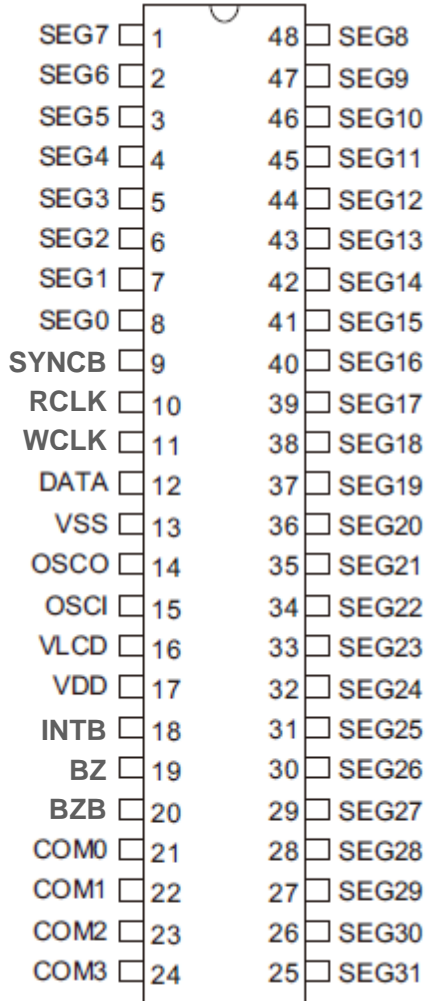
6.3 NY9L070x

N/A

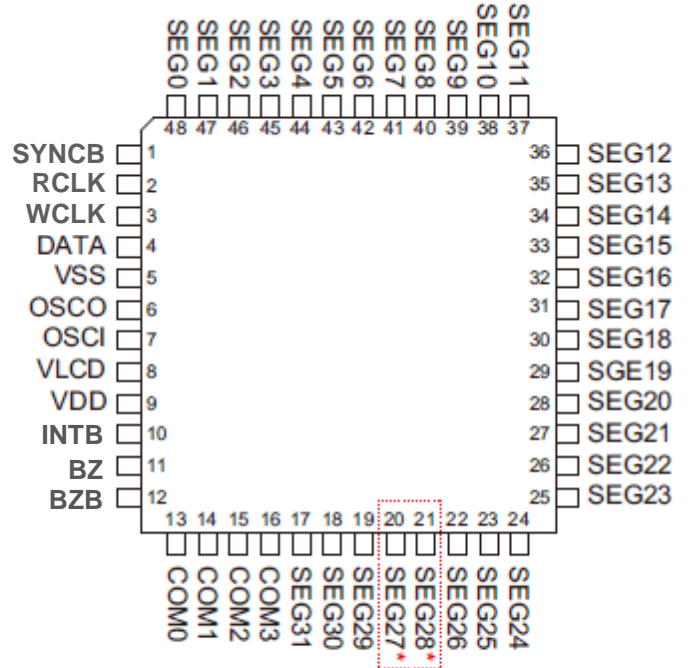
**7. Package Pin Definition**

**7.1 NY9L010A**

**(a) NY9L010AS48 (SSOP-48)**



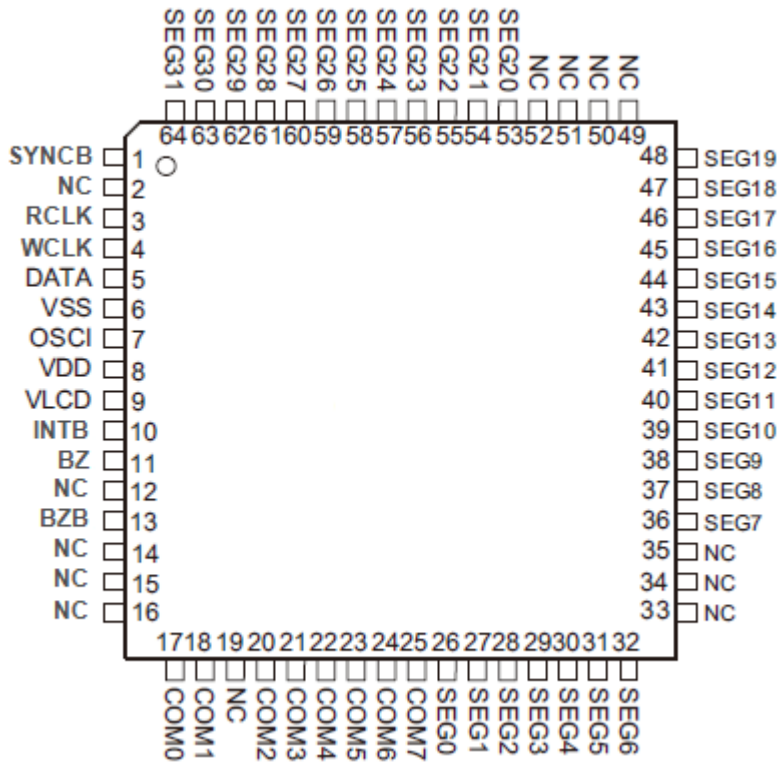
**(b) NY9L010AQ48 (LQFP-48, 7mmx7mm)**



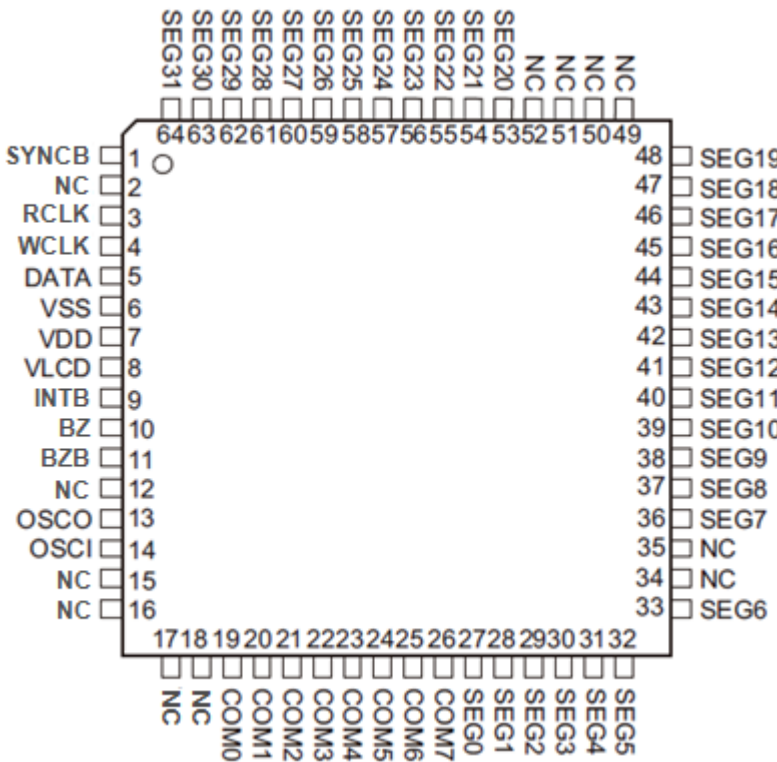
**Note: For LQFP48 package, the SEG27 and SEG28 are not in sequential order.**

7.2 NY9L020x

(a) NY9L020AQ64 & NY9L020BQ64 (7mm x 7mm)



(b) NY9L020CQ64 & NY9L020DQ64 (7mm x 7mm)

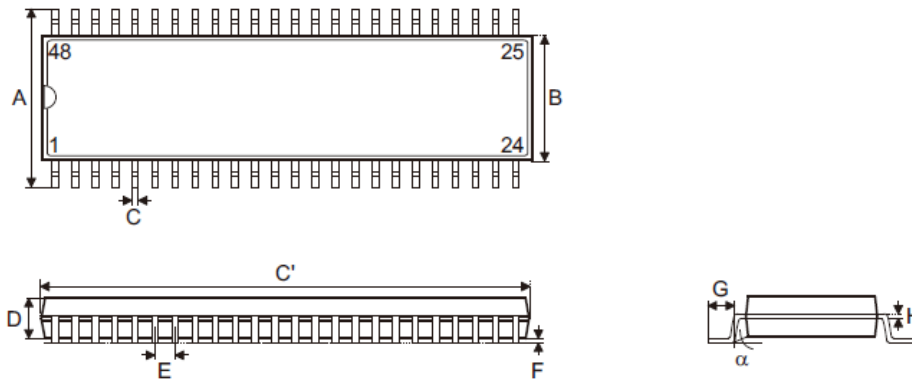


7.3 NY9L070x

N/A

**8. Package Dimension**

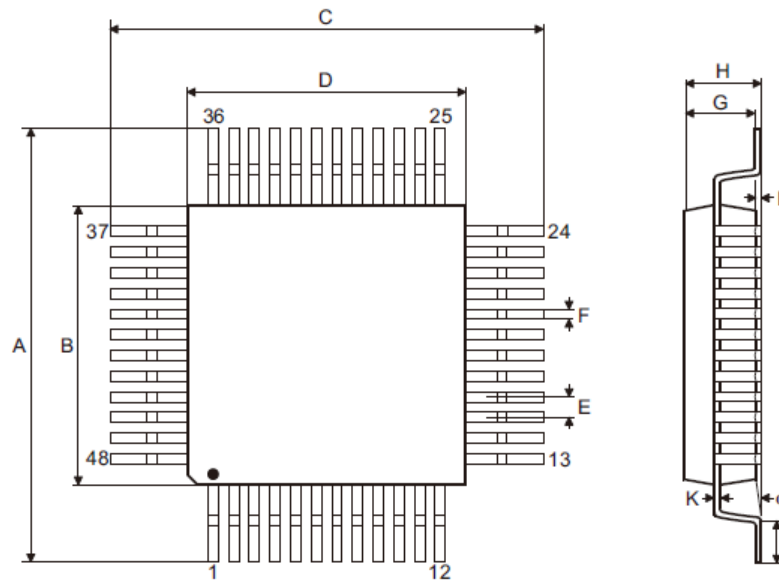
**8.1 SSOP-48 (300 mil)**



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.395	—	0.420
B	0.291	—	0.299
C	0.008	—	0.014
C'	0.620	—	0.630
D	0.095	—	0.110
E	—	0.025	—
F	0.008	—	0.016
G	0.020	—	0.040
H	0.005	—	0.010
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	10.03	—	10.67
B	7.39	—	7.59
C	0.20	—	0.34
C'	15.75	—	16.00
D	2.41	—	2.79
E	—	0.64	—
F	0.20	—	0.41
G	0.51	—	1.02
H	0.13	—	0.25
α	0°	—	8°

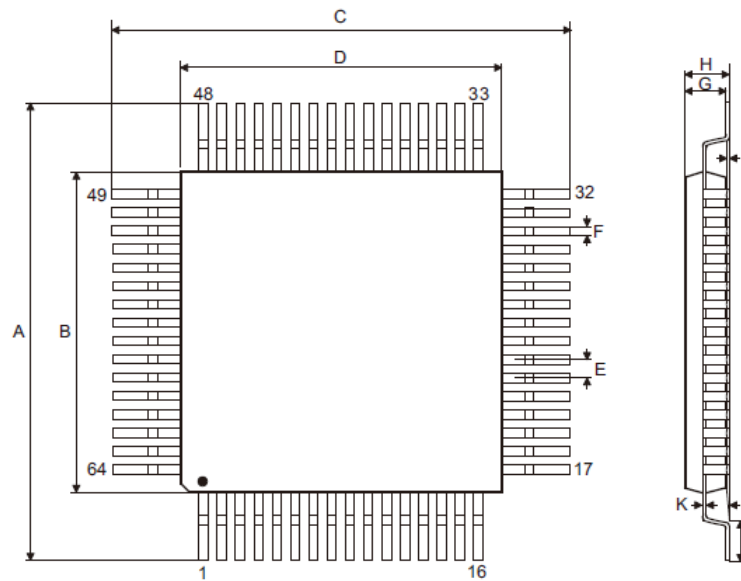
**8.2 LQFP-48 (7mm x 7mm)**



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.350	—	0.358
B	0.272	—	0.280
C	0.350	—	0.358
D	0.272	—	0.280
E	—	0.020	—
F	—	0.008	—
G	0.053	—	0.057
H	—	—	0.063
I	—	0.004	—
J	0.018	—	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	8.90	—	9.10
B	6.90	—	7.10
C	8.90	—	9.10
D	6.90	—	7.10
E	—	0.50	—
F	—	0.20	—
G	1.35	—	1.45
H	—	—	1.60
I	—	0.10	—
J	0.45	—	0.75
K	0.10	—	0.20
α	0°	—	7°

**8.3 LQFP-64 (7mm x 7mm)**



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.350	—	0.358
B	0.272	—	0.280
C	0.350	—	0.358
D	0.272	—	0.280
E	—	0.016	—
F	0.005	—	0.009
G	0.053	—	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	—	0.030
K	0.004	—	0.008
$\alpha$	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	8.90	—	9.10
B	6.90	—	7.10
C	8.90	—	9.10
D	6.90	—	7.10
E	—	0.40	—
F	0.13	—	0.23
G	1.35	—	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	—	0.75
K	0.09	—	0.20
$\alpha$	0°	—	7°



8.4 LQFP-100 (10mm x 10mm)

N/A

**9. Ordering Information**

<b>P/N</b>	<b>Shipping Type</b>	<b>Remarks</b>
NY9L010A	Die	--
NY9L010AS48	SSOP-48	Width 300 mil.
NY9L010AQ48	LQFP-48	7mm x 7mm
NY9L020A	Die	Built-in OSC w/o LDO
NY9L020AQ64	LQFP-64	7mm x 7mm
NY9L020B	Die	Built-in OSC w/ LDO
NY9L020BQ64	LQFP-64	7mm x 7mm
NY9L020C	Die	External X'tal w/o LDO
NY9L020CQ64	LQFP-64	7mm x 7mm
NY9L020D	Die	External X'tal w/ LDO
NY9L020DQ64	LQFP-64	7mm x 7mm
NY9L070A	Die	w/o LDO
NY9L070AQ100	LQFP-100	10mm x 10mm
NY9L070B	Die	w/ LDO
NY9L070BQ100	LQFP-100	10mm x 10mm

*\* NY9L070x is not available till Dec. 2016.*