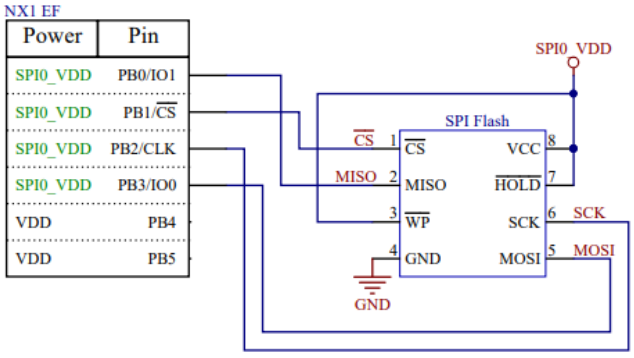
Application Notices for NX1 Series IC Using SPI Flash

Description: There are some constraints and limitations for developing NX1 applications with SPI Flash.

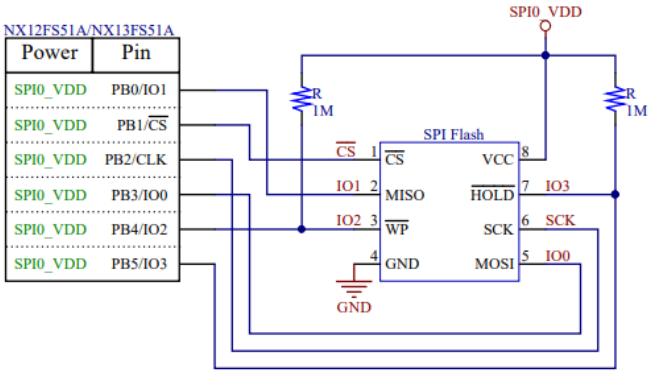
1. Programming Tool of NX1

1-1 There are limitations in capacity of current hardware programming tools. The maximum programming capacity of SPI Flash in OTP_Writer (Ver. C) is 16Mbits, and NX_Programmer is 256Mbits that must work with NX1 OTP. If SPI FLASH 256Mbits works with NX1 OTP, please program OTP via Smart_Writer Ver. A with Q-Writer 4.30 Beta SPI Flash(XMC) 256M [Build 200916.00], and it's only for online development and programming. If it needs to program SPI Flash with larger capacity, please use a third-party tool.

1-2. NX1 series IC four-wire communication connects SPI Flash, the status of SPI Flash /WP and /HOLD pin will vary depending on the design of each brands. Some brands may cause programming failure or read and write errors. To avoid the above situations, it is recommended that a pull-up voltage SPI0_VDD must be connected. The diagram is as follows.



1-3. NX12FS51A / NX13FS51A six-wire communication connects SPI Flash. When the user executes the ICP for first time, and never sets QE bit for SPI Flash (Enable Quad mode), NX12FS51A / NX13FS51A will set PB4 and PB5 as floating in the program mode, the SPI Flash of some brands may cause programming failure or read and write errors. To avoid the above situations, it is recommended to connect /WP(IO2) and /HOLD(IO3) pin with a pull-up resistor. The diagram is as follows.



2. Development Tools of NX1

2-1. For NX1_FDB, the maximum capacity of SPI Flash is 256Mbits, and 256Mbits supports Winbond W25Q256FV only. User must keep 1Mbits from the SPI Flash of NX1 FDB so that NX1 EV chip can emulate OTP ROM, the actual SPI Flash capacity of NX1 FDB for development should deduct 1Mbits.

Note: The SPI Flash of NX1_FDB version between Ver.B 2018/9/7 and Ver.C 2020/5/8 is a special OEM version, and its actual capacity is twice the capacity shown on the FDB.

2-2. The EV chip on NX1_FDB version which is before the NX1_FDB Ver.B 2018/08/06 will execute a boot code in Quad mode to load user code after power on. In order to comply with the NX1_FDB boot procedure, the replaced SPI Flash must support the Quad mode.

2-3. NX11P2xAB development board only supports Single and Dual mode, not Quad mode. That is, the WP and Hold pins of SPI Flash are not connected to PB4 and PB5, instead, they are connected to SPI0_VDD to pull High. If users select the Quad mode for developing programs, data cannot be received correctly.

3. Program Development

3-1. The settings of SPI Flash QE bit are varied in the status register of each brand. It will consume more system resources to support various SPI Flash brands, and it is not possible to cover all of them. Therefore, when selecting 1-4-4 (Quad mode) in C_Module or *Q-Code*, the program will check if SPI Flash is the Brand of Winbond(Mfr ID: 0xEF), MXIC(Mfr ID: 0xC2), PUYA(Mfr ID:0x85) or Nyquest N25Q series(Mfr ID: 0x20,0x1F) and sets QE bit accordingly. If user replaces the SPI Flash, QE bit will not be set, and the Quad mode may fail. *Q-Code* cannot power on, and needs to set the QE bit manually. The methods of setting the QE bit manually are illustrated as follows.

Example:

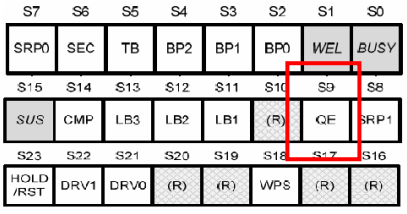
Q-Code can read/write SPI Flash status register on "**Before_PowerOn**" path to set QE bit.

SPI_WRSR(VAR8 reg,VAR32 data, VAR8 len)

SPI_RDSR(VAR8 reg,VAR16 data)

To take Winbond as example, there are 2 situations:

A). **Before_PowerOn**: SPI_WRSR(0x31,0x2),SPI_RDSR(0x35,ReadSts2)



Data Input Output	Byte 1	Byte 2
Clock Number	(0 – 7)	(8 – 15)
Read Status Register-1	05h	(S7-S0)[2]
Write Status Register-1[4]	01h	(S7-S0)[4]
Read Status Register-2	35h	(S15-S8)[2]
Write Status Register-2	31h	(S15-S8)
Read Status Register-3	15h	(S23-S16)[2]
Write Status Register-3	11h	(S23-S16)

B). **Before_PowerOn**: SPI_WRSR(0x1,0x200,2),SPI_RDSR(0x35,ReadSts2)

S7	S6	S5	S4	S3	S2	S1	S0
SRP0	SEC	TB	BP2	BP1	BP0	*WEL*	*BUSY*
S15	S14	S13	S12	S11	S10	S9	S8
SUS	CMP	LB3	LB2	LB1	(R)	QE	SRP1
S23	S22	S21	S20	S19	S18	S17	S16
HOLD /RST	DRV1	DRV0	(R)	(R)	WPS	(R)	(R)

Command Name	Byte 1	Byte 2	Byte 3
Read Status Register	05H	(S7-S0)	
Read Status Register-1	35H	(S15-S8)	
Write Status Register	01H	S7-S0	S15-S8

To take MXIC as example:

Before_PowerOn: SPI_WRSR(0x1,0x40),SPI_RDSR(0x15,ReadSts2)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SRWD (Status Register Write Disable)	QE (Quad Enable)	BP3 (level of protected block)	BP2 (level of protected block)	BP1 (level of protected block)	BP0 (level of protected block)	WEL (write enable latch)	WIP (write in progress bit)

3-2. In *Q-Code* and C_Module, NX11PxxA or NX11M2xA will issue deep power down command to SPI Flash and shut down the power from SPI0_VDD when entering Halt mode. When waking up, it will power on and then issue release deep power down command. When the power is on, there is a time to get to the working voltage. Each SPI Flash has different working voltage, so the time of SPI0_VDD to reach the working voltage is also different. For example, Winbond W25Q64FV takes about 5ms. Currently, the program of *Q-Code* and C_Module implement a 15ms delay before executing any commands, and it should be enough for most of the SPI flash to wake up from release deep power down mode, however, there are many SPI Flash brands, and user should be aware of this issue if SPI Flash is replaced.

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
VCC (min) to /CS Low	tVSL	20		µs
Time Delay Before Write Instruction	tPUW	5		ms
Write Inhibit Threshold Voltage	VWI	1.0	2.0	V

Note:

1. These parameters are characterized only.

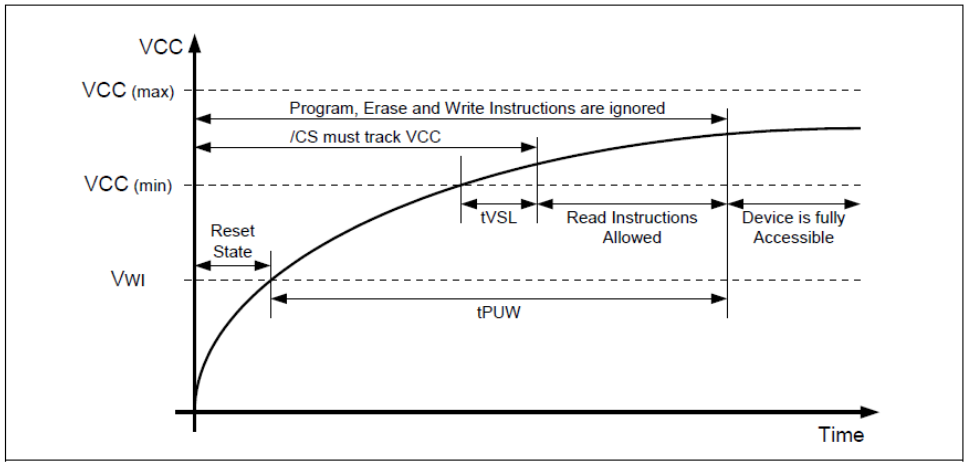


Figure 58. Power-up Timing and Voltage Levels

3-3. The XIP (eXecute In Place) and XIP COC (Common OTP Code) functions have to use Quad mode (1-4-4) because of processing speed.

3-4. Because of processing speed, it's recommended to use Quad mode (1-4-4) for VR (Voice Recognition) applications.