Application Notice for NX1 EF Series IC Using SPI Flash Circuit

Description: When the NX1 EF series IC used SPI Flash, the power of SPI communication port has to be modified to work with the external Flash circuit.

Reason: **For NX1 EF series IC, SPI0_VDD or VDD provides the power to the communication port of SPI0 and SPI1 according to the settings of *NYIDE / Q-Code.*** The external circuit must be modified by this application notice to avoid potential mismatch and cause hardware abnormalities. The SPI0 setting (*NYIDE* / *Q-Code*) please refer to the Table 1. The SPI 1setting (*NYIDE*) please refer to Table 2.

Table 3. SPI0 Setting with *NYIDE* / *Q-Code*

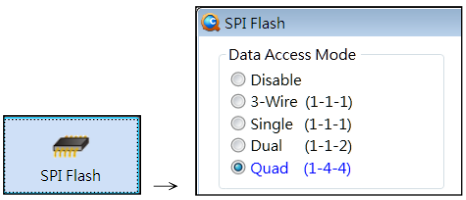
	Descriptions	**Remarks**
NYIDE	(project file path)…\src\nx1_config.h 674 #define _SPI_MODULE ENABLE 675 #if _EF_SERIES 676 #define _SPI_ACCESS_MODE SPI_1_4_4_MODE 677 #else	The available options for **_SPI_ACCESS_MODE:** SPI_1_1_1_MODE SPI_1_2_2_MODE SPI_1_4_4_MODE SPI_1_1_2_MODE SPI_1_1_1_MODE_3WIRE *NYIDE* will modify the power of SPI0 communication port automatically according to **_SPI_MODULE** and **_SPI_ACCESS_MODE**.
Q-Code	Option → SPI Flash → Data Access Mode 	*Q-Code* 依 will modify the voltage source of SPI0 communication port according to the setting of **Data Access Mode**.

Table 4. SPI1 Setting with *NYIDE*

	Descriptions	**Remarks**
NYIDE	(project file path)…\src\nx1_config.h 687 #define _SPI1_MODULE DISABLE 688 #define _SPI1_USE_FLASH DISABLE 689 #define _SPI1_ACCESS_MODE SPI_1_1_1_MODE_3WIRE	The available options for **_SPI1_ACCESS_MODE**: SPI_1_1_1_MODE SPI_1_2_2_MODE SPI_1_1_2_MODE

		SPI_1_1_1_MODE_3WIRE *NYIDE* will modify the power of SPI1 communication port automatically according to **_SPI1_MODULE** and **_SPI1_ACCESS_MODE**.

In the application development stage, the SPI communication protocol of *NYIDE/Q-Code* must be followed to find out the appropriate SPI application circuit.

For *NYIDE* with SPI0, please refer to Table 5.

For *NYIDE* with SPI1, please refer to Table 6.

For *Q-Code* with SPI0, please refer to Table 7.

Table 5. *NYIDE* with SPI0 communication protocol and application circuit.

SPI0 Communication Protocol		SPI0 application circuit
_SPI_MODULE	**_SPI_ACCESS_MODE**	
DISABLE		SPI0 disable
ENABLE	SPI_1_1_1_MODE_3WIRE	SPI0 three-wire communication
	SPI_1_1_1_MODE	SPI0 four-wire communication
	SPI_1_1_2_MODE	
	SPI_1_2_2_MODE	
	SPI_1_4_4_MODE	SPI0 six-wire communication

Table 6. *NYIDE* with SPI1 communication protocol and application circuit.

SPI1 Communication Protocol		SPI1 application circuit
_SPI1_MODULE	**_SPI1_ACCESS_MODE**	
DISABLE		SPI1 disable
ENABLE	SPI_1_1_1_MODE_3WIRE	SPI1 three-wire communication
	SPI_1_1_1_MODE	SPI1 four-wire communication
	SPI_1_1_2_MODE	
	SPI_1_2_2_MODE	

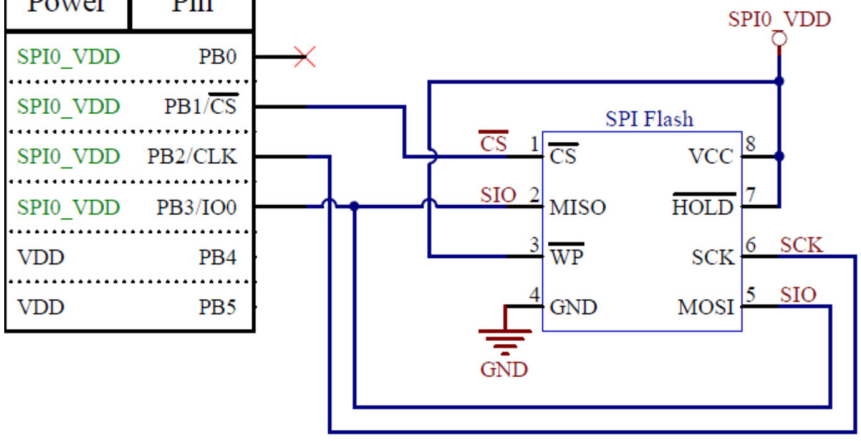
Table 7. *Q-Code* with SPI0 communication protocol and application circuit.

SPI0 Communication Protocol	SPI0 application circuit
Data Access Mode	
Disable	SPI0 disable
3-Wire(1-1-1)	SPI0 three-wire communication
Single(1-1-1)	SPI0 four-wire communication

Dual(1-1-2)	
Quad(1-4-4)	SPI0 six-wire communication

Solution: For SPI0 and SPI1 application circuit and their description, please refer Table 8 with SPI0 and Table 9 with SPI1 to modify the circuit.

Table 8. SPI0 application circuit.

<table>
<tr>
<td>SPI0 disable</td>
<td>NX1 EF
<table>
<tr><th>Power</th><th>Pin</th></tr>
<tr><td>VDD</td><td>PB0</td></tr>
<tr><td>VDD</td><td>PB1</td></tr>
<tr><td>VDD</td><td>PB2</td></tr>
<tr><td>VDD</td><td>PB3</td></tr>
<tr><td>VDD</td><td>PB4</td></tr>
<tr><td>VDD</td><td>PB5</td></tr>
</table>
※VDD provides power to PB0 ~ PB5 that can be converted as GPIO usage.</td>
</tr>
<tr>
<td>SPI0 three-wire communication</td>
<td>NX1 EF
<table>
<tr><th>Power</th><th>Pin</th></tr>
<tr><td>SPI0_VDD</td><td>PB0</td></tr>
<tr><td>SPI0_VDD</td><td>PB1/$\overline{CS}$</td></tr>
<tr><td>SPI0_VDD</td><td>PB2/CLK</td></tr>
<tr><td>SPI0_VDD</td><td>PB3/IO0</td></tr>
<tr><td>VDD</td><td>PB4</td></tr>
<tr><td>VDD</td><td>PB5</td></tr>
</table>


※PB0 is powered by SPI0_VDD. Please check the voltage level when using it. It is recommended to keep it as a reserved pin.
1. If PB0 is set as Input, the internal pull-up resistor will be invalid, and cause PB0 cannot wake up the sleep IC.
2. If PB0 is set as Output, please check the level, and the output will pause when IC is sleeping.
※VDD provides power to PB4 and PB5 that can be converted as GPIO usage.</td>
</tr>
</table>

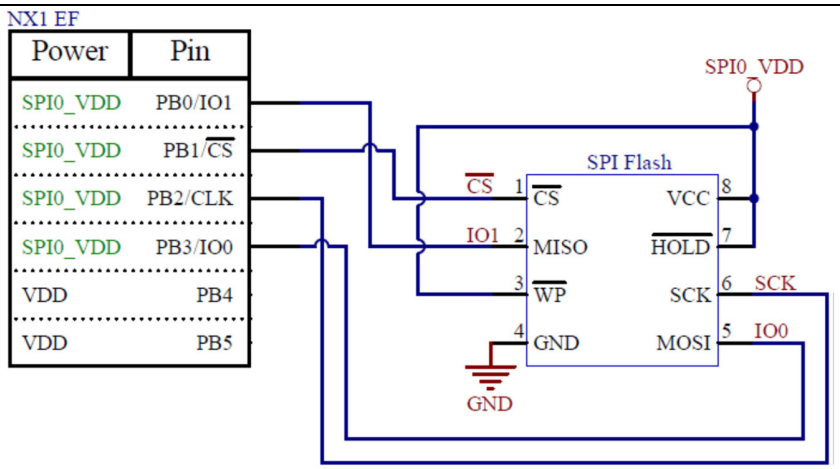
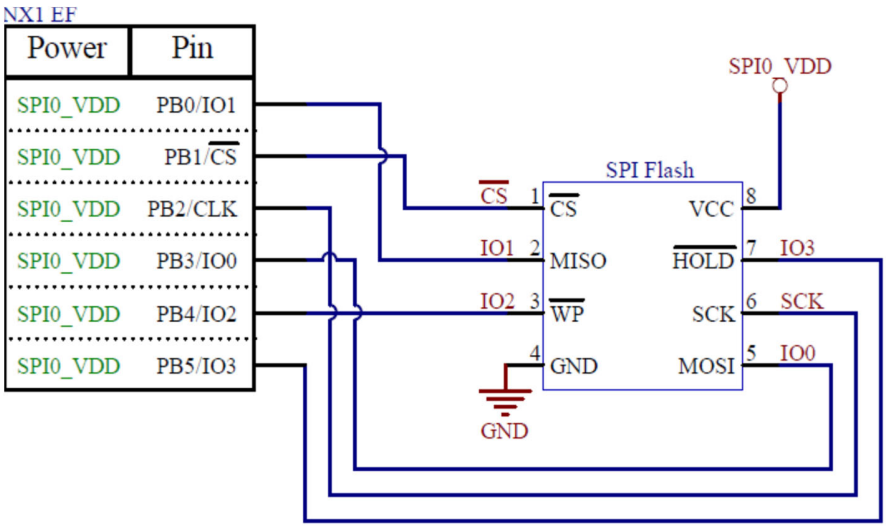
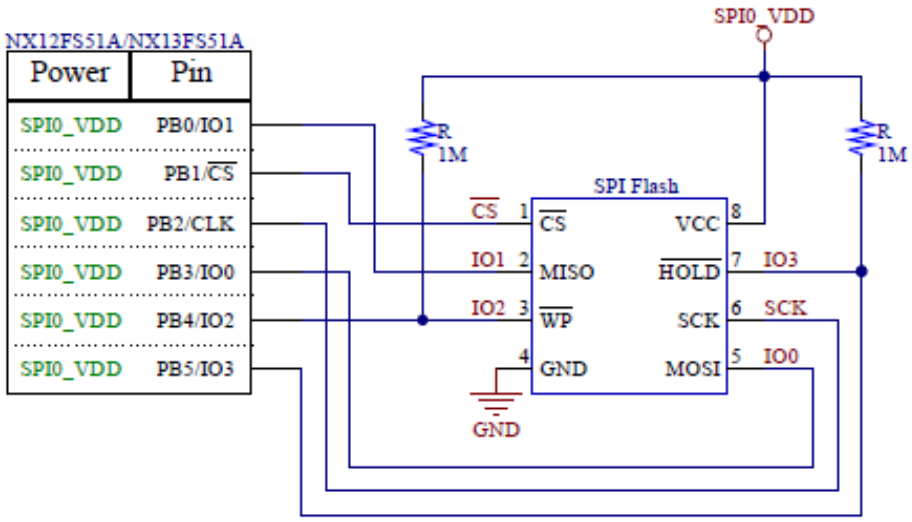
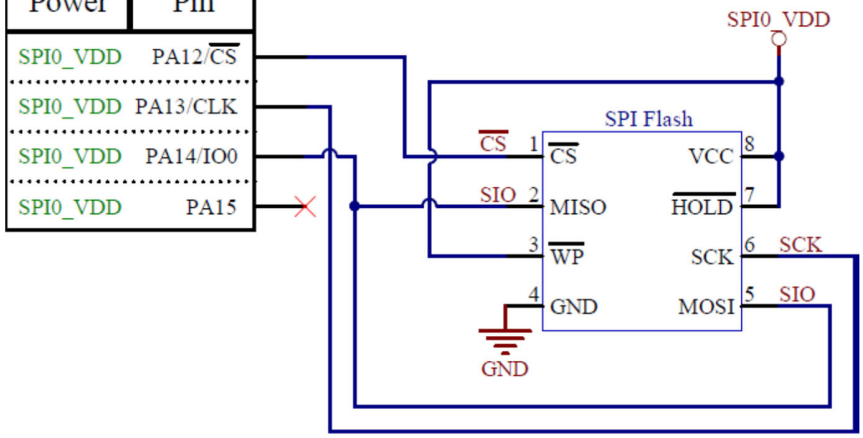
SPI0 four-wire communication	 ※VDD provides power to PB4 and PB5 that can be converted as GPIO usage.
SPI0 six-wire communication	  ※For NX12FS51A and NX13FS51A to program normally, PB4 and PB5 must connect a pull-up resistor. For details, please refer to AP-27.

Table 9. SPI1 application circuit

SPI1 disable	NX1 EF Power / Pin VDD PA12 VDD PA13 VDD PA14 VDD PA15 ※VDD provides power to PA12 ~ PA15 that can be converted as GPIO usage.
SPI1 three-wire communication	NX1 EF Power / Pin SPI0_VDD PA12/$\overline{CS}$ SPI0_VDD PA13/CLK SPI0_VDD PA14/IO0 SPI0_VDD PA15  ※PA15 is powered by SPI0_VDD. Please check the voltage level when using it. It is recommended to keep it as a reserved pin. 1. If PA15 is set as Input, the internal pull-up resistor will be invalid, and cause PA15 cannot wake up the sleep IC 2. If PA15 is set as Output, please check the level, and the output will pause when IC is sleeping.
SPI1 four-wire communication	NX1 EF Power / Pin SPI0_VDD PA12/$\overline{CS}$ SPI0_VDD PA13/CLK SPI0_VDD PA14/IO0 SPI0_VDD PA15/IO1