



九齊科技股份有限公司
Nyquest Technology Co., Ltd.

DATA SHEET

NX11FS2x (EF Series)

32-bit Audio SoC for SBC / MIDI Playback & Effect Processing

Version 1.5

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Revision History

Version	Date	Description	Modified Page
1.0	2023/2/24	Formal release.	-
1.1	2023/3/16	1. Add multi-function for PB4 / PB5 to support Quad I/O mode. 2. Rename pin names for programming interface to avoid confusion.	5, 13, 27 12, 13, 27
1.2	2023/11/23	1. Update PWM-IO pin for NX11FS21A / NX11FS20A. 2. Update trim accuracy for I_HRC and I_LRC. 3. Add test result of FCC part 15B. 4. Add DC characteristics for LVR.	6, 7, 9, 10, 12, 13, 14, 26, 27
1.3	2024/01/11	1. Add note for IR wake-up application. 2. Add note for the use of decoupling capacitor in application circuit.	22, 26
1.4	2024/08/15	1. Add NX11FS2HA.	5, 6, 7, 9, 10, 14, 16, 22, 27, 30
1.5	2025/07/25	1. Add reliability info of Embedded Flash. 2. Revise max. SPI clock speed. 3. Add notes for Application Circuit. 4. Revise Package Pin Description.	6, 10, 7, 11, 28, 29

TABLE OF CONTENTS

1. 概述	5
2. 功能	6
1. GENERAL DESCRIPTION.....	9
2. FEATURES	10
3. BLOCK DIAGRAM.....	13
4. PAD / PIN DESCRIPTION.....	14
5. FUNCTIONAL DESCRIPTION.....	16
5.1 Memory Organization	16
5.2 Clock Generator	16
5.3 Operating Mode.....	17
5.4 Interrupt.....	17
5.5 Peripherals	17
5.5.1 I/O Port	17
5.5.2 SPI.....	18
5.5.3 UART	18
5.5.4 PWM-IO.....	18
5.6 Timer	18
5.7 Software CapTouch.....	19
5.8 IR TX	20
5.9 RTC.....	20
5.10 WDT	20
5.11 DAC & Audio PWM Driver	21
5.12 LVD	21
5.13 Options.....	22
6. ELECTRICAL CHARACTERISTICS.....	23
6.1 Absolute Maximum Rating.....	23
6.2 DC Characteristics.....	23
6.3 DAC Characteristics	25
6.4 Audio PWM Characteristics	25
6.5 Frequency vs. Voltage.....	26
6.5.1 I_HRC.....	26

6.5.2	I_LRC	26
6.6	Frequency vs. Temperature.....	27
6.6.1	I_HRC.....	27
6.6.2	I_LRC	27
7.	APPLICATION CIRCUIT	28
8.	PACKAGE PIN ASSIGNMENT	29
8.1	SOP-8 (150mil, 1.27mm pin pitch).....	29
8.2	SOP-16 (150mil, 1.27mm pin pitch).....	29
8.3	SSOP-24 (150mil, 0.635mm pin pitch).....	30
9.	PACKAGE DIMENSION	31
9.1	SOP-8 (150mil, 1.27mm pin pitch).....	31
9.2	SOP-16 (150mil, 1.27mm pin pitch).....	31
9.3	SSOP-24 (150mil, 0.635mm pin pitch).....	32
10.	ORDERING INFORMATION	33

1. 概述

NX11FS2x 是基於 32 位元 MCU 的高品質 Speech/MIDI 系統單晶片處理器，特別設計用來處理數位語音相關的功能。NX11FS2x 源自 NX1 OTP 系列，其在 Speech/MIDI 播放的各類應用，早已廣為業界所採用。NX11FS2x 為新一代的 EF (Embedded Flash，嵌入式快閃記憶體) 系列，用來彌補一次性燒錄 OTP 之不足，並且將 ICE 偵錯功能直接集成在量產晶片之中，使得開發流程更加地簡化、順暢。相較於掩膜 (Mask ROM) 產品而言，NX11FS2x 則具有絕佳的 MOQ 和交期的優勢。

NX11FS2x 採用記憶體映射架構，最高可以定址到 16MB，包含記憶體 (EF/RAM)、週邊、以及 SPI Flash 的儲存空間 (支援 Bank 擴充以及指令/資料模式)。由於 DSP 演算法以及硬體規格的提升，NX11FS2x 支援 SBC (Sub-Band Coding, 子帶編碼)，相較於傳統式的 ADPCM 演算法，除了更高的壓縮率之外，在音質上也大幅超越傳統的語音水準！NX11FS2x 內建 ILM/DLM 本地匯流排，具有單一週期乘法器及七週期除法器，再加上 32 位元 CPU 的高性能運算，可以用來實現豐富的 8 和絃 MIDI。所有的資料，包括 SBC / MIDI 檔案、音色波表 (Wavetable)、XIP 本地執行程式、以及一般使用者的資料，除了內建的 EF 之外，也都可以存放到 SPI Flash。

內建 40MHz 高頻以及 32KHz 低頻的雙時脈設計，可讓使用者在 Normal / Standby / Halt 模式之間切換以求取最佳的功耗/效能比、抑或在低耗能情況下，作為計時之用途。NX11FS2x 除了內建 0.5Mb / 1Mb / 2Mb / 4Mb / 8Mb 的 EF (嵌入式快閃記憶體) 之外，也可以藉由外接的 SPI Flash 來擴充記憶體大小。

NX11FS2x 涵蓋了大量實用的功能：2 組 16 位元的計時器 (Timer)；最多 8 通道硬體 PWM-IO 輸出；14 位元的數位類比轉換器 (DAC) 外接功放，或者選擇內建的 $\Sigma\text{-}\Delta$ PWM 來直接驅動喇叭；每根 I/O 管腳獨立控制、可作為多功能用途的 GPIO；支援 38KHz/57KHz/125KHz/500KHz 載波傳輸的紅外發射 (IR TX) 或 QFID 應用；SPI0 用來控制外部的 SPI Flash，並支援 Single/Dual/Quad I/O 模式以及 XIP (eXecute In Place，在地執行程式) 功能；UART 可作為 ISP (在系統燒錄) 的來源，串列傳輸的介面，或者用來連接超級終端作為簡易的除錯工具。

NX11FS2x 系列除了可用 C 語言在 *NYIDE* 環境下開發，提供客戶更多的控制度來滿足較複雜的產品開發以外，更將高階的 *Q-Code* 語言移植到 32 位元 MCU，不僅提供簡單易用和高生產力的開發環境，更把握了產品構想及時實現的重要性。NX11FS2x 內建仿真線路，可以在實際量產的晶片進行程式除錯，以完成原型的演示，並進而直接量產。在大量生產的時候，可以使用 ICP (In-Circuit Programming，在線燒錄) 的功能，方便客戶先組裝 PCBA 再進行燒錄 EF 以及量產板上的 SPI Flash。另外，透過 ISP 的功能，客戶則可以在成品上做到程式以及內容的更新。

NX11FS2x 系列提供多種封裝型式來滿足各式多樣化的應用：SOP-8、SOP-16、SSOP-24。

2. 功能

- 寬廣的工作電壓：2.0V ~ 5.5V
 - CPU 最高速度 40MHz 運行時，最低工作電壓為 2.0V。
- 32 位元 CPU 內核
 - Andes N705-S，性能相當於 ARM Cortex-M0+。
 - 最高 CPU 頻率：40MHz，搭配 1 個等待狀態 (wait-state) 的高速 20MHz EF 存取。
 - 單一指令週期快速乘法器，七指令週期快速除法器。
 - 本地指令/資料記憶體匯流排。
- 共有 5 個單芯片封裝的母體。

P/N	VDD	RAM	EF	Duration (Sec)		I/O	SPI 0	UART	16-bit Timer	PWM -IO	Dual Clock	Cap Touch	DAC	Power Amp.	IR Tx	IR Wakeup	LVD	OCD	Package
				16Kbps	24Kbps														
NX11FS2HA	2.0V ~ 5.5V	4KB	0.5Mb	25	16	4 12	- v	v	2	1 3	v	v	-	Σ-Δ PWM	v	HW	v	-	SOP-8 SOP-16
NX11FS20A	2.0V ~ 5.5V	4KB	1Mb	57	38	4 12	- v	v	2	1 3	v	v	-	Σ-Δ PWM	v	HW	v	-	SOP-8 SOP-16
NX11FS21A	2.0V ~ 5.5V	4KB	2Mb	123	82	4 12	- v	v	2	1 3	v	v	-	Σ-Δ PWM	v	HW	v	-	SOP-8 SOP-16
NX11FS22B	2.0V ~ 5.5V	4KB	4Mb	254	169	4 12 20	- v v	v	2	1 7 8	v	v	-	Σ-Δ PWM	v	HW	v	v	SOP-8 SOP-16 SSOP-24
NX11FS23A	2.0V ~ 5.5V	4KB	8Mb	516	344	4 12 20	- v v	v	2	1 7 8	v	v	14-bit	Σ-Δ PWM	v	FW	v	v	SOP-8 SOP-16 SSOP-24

Table 1 NX11FS2x 選型表

- 內建 0.5Mb ~ 8Mb 高可靠性、嵌入式快閃記憶體
 - 10 年資料保存期
 - 100K 擦除/編程次數
 - 程序/聲音內容之儲存空間
- 內建 4KB RAM
- 雙時脈操作，內建 I_HRC (40MHz) 和 I_LRC (32,768Hz) 振盪器。(出廠精準度調校：I_HRC @ +/-1.0%，I_LRC @ +/-3.0%)
- 三種工作模式可隨系統需求調整電流消耗：正常 (Normal) / 待機 (Standby) / 睡眠 (Halt)，在睡眠模式下，典型耗電流 2uA @ 5.5V。
- 內建 8 階低電壓檢測器 (LVD)：3.6V, 3.4V, 3.2V, 3.0V, 2.8V, 2.4V, 2.2V, 2.0V，出廠調校參考電壓 3.4V 至 +/-3% 精準度。
- 內建低壓復位功能 (LVR)。
- 兩組具備各式時鐘源的 16 位下數計時器 (Timer0 / Timer1)。
- 內建 14 位元 DAC (數位類比轉換器)，可以外接功放。(僅限 NX11FS23A)
- 內建 13 位元 Σ-Δ PWM 功放，可以直接驅動喇叭。
- 最多 20 根 I/O 管腳，除了上拉電阻大小與 Sink 電流以 byte 為單位選擇以外，每根管腳之組態皆可由暫存器個別位元控制，並可經由暫存器設定多功能用途。

- SPI0 主模式，可用來連接 SPI Flash
 - 高達 32MHz 時脈。
 - 支援 32 位元模式，可定址超過 128Mb。
 - 支援數據模式以及 XIP 模式 (在地執行程式)。
 - 支援 x1 / x2 / x4 I/O 模式 (Single / Dual / Quad)。
- 支援 IR TX (可選 Timer 0 / 1)
- 支援實時時鐘 (RTC)：可選 16.384KHz / 1.024KHz / 64Hz / 2Hz 中斷。
- 支援看門狗 (WDT) 計時：可選 188ms / 750ms 重置。
- 支援 ISP (In-System Programming，在系統燒錄)
 - 來源: UART
 - 目的地: EF, SPI Flash (經由程式控制)
 - ISP boot 程式保護機制
- 支援硬體 UART
 - 全雙工 TX/RX，具 1-level FIFO
 - 傳輸率 (Baud Rate) 支持 115,200 / 230,400 / 460,800 / 1Mbps
- 兩組 PWM-IO 產生器 (PWMA / PWMB)
 - 每組最多 4 個獨立的 PWM-IO 通道 (PWMA0 ~ PWMA3 / PWMB0 ~ PWMB3)。
 - 每組 PWM-IO 產生器擁有一個具備各式時鐘源的 16 位元計時器 (可獨立當作一般計時器使用)。
 - 每根 PWM-IO 管腳具有獨立的 16 位元脈寬暫存器。
 - NX11FS2HA / NX11FS20A / NX11FS21A 只有一組 PWM-IO 產生器 (PWMA)。
- 支援電容式觸摸感測 (CapTouch Sensor)
 - 所有的 PA 腳位皆可選擇作為觸摸鍵
- 支援 EF 安全保護機制。
- 簡單易用的開發環境
 - 高階的 *Q-Code* 程式。
 - 進階的 *NYIDE C-Module* 程式。
 - 內建兩根管腳的 OCD (On-Chip Debugger) 仿真線路，支援 *Q-Code* / *C-Module* 源代碼仿真。
(NX11FS2HA / NX11FS20A / NX11FS21A 除外)
 - 多用途 NX_Programmer 作為仿真以及 EF/SPI Flash 燒錄之工具。
 - Smart Writer 作為封裝片量產之 EF/SPI Flash 代燒，或者 ICP (在線燒錄) 之用途。
 - 6 根管腳的燒錄介面 (VDD, VSS, PD0, PD1, PA12, RSTB/PA8)。
- 基於軟件的 Speech/MIDI 解碼器以及各式演算法
 - ADPCM 解碼：4 通道，每採樣點 4 位元 / 5 位元。
 - SBC 解碼：1 通道，4.5K ~ 32Kbps (位元速率)，最高頻寬 16KHz。

- MIDI 解碼：最多 8 通道 (32KHz 輸出採樣率)。
- 播放特效：變速不變調、變調不變速等等。
- 支援 4 ~ 32 倍頻超採樣濾波器。
- 出貨形態
 - 封裝片：SOP-8 / SOP-16 / SSOP-24

1. GENERAL DESCRIPTION

The NX11FS2x is a 32-bit MCU based high-quality speech/MIDI SoC, which is specially designed for various audio-related DSP applications. Its predecessor, the NX1 OTP series, has been well accepted in the market for numerous applications like long-duration speech, voice prompt, and MIDI synthesis. The NX1 Embedded Flash (EF) series follows the same architecture but uses EF to replace the OTP memory core and embeds OCD (On-Chip Debugger) at production chips to make the project development much easier than ever. As compared with mask ROM counterparts, the NX11FS2x got absolute advantage over MOQ and lead time.

The NX11FS2x got memory-mapped architecture, which can address up to 16MB space that includes memory (EF / RAM), register files, peripheral and SPI Flash (that supports Bank for expansion and Instruction / Data modes). The highly compressed SBC (Sub-Band Coding) is achieved with greatly enhanced quality & much less memory size compared against traditional ADPCM coding due to the incorporation of efficient DSP algorithms as well as the upgrade of H/W spec. By incorporating Instruction / Data local buses, 1-cycle multiplier and 7-cycle divider for the 32-bit N705-S core, it reaches outstanding performance when the system clock runs at 40MHz. The S/W-based MIDI synthesizer can reach more than 8 polyphonic channels, with all data including SBC / MIDI files, wavetable timbres, XIP (eXecutable In Place) program code and general user data stored in the embedded Flash and/or external SPI Flash memory.

The dual clock design with built-in 40MHz I_HRC and 32KHz I_LRC gives users the freedom to switch among Normal / Standby / Halt modes for the balance of power consumption and performance or to keep the time under low power condition. Set aside the EF inside the NX11FS2x, users may incorporate external SPI Flash as well to expand the memory easily.

There are various useful features inside the NX11FS2x: Two sets of 16-bit Timers; up to 8-ch H/W PWM-IO pins; 14-bit DAC to connect with external power amplifier or built-in $\Sigma\Delta$ PWM amplifier to drive speaker directly; independently configurable GPIO per pin with alternate functions; IR TX that supports 38KHz / 57KHz / 125KHz / 500KHz carrier for Infrared or QFID applications; SPI0 to connect with external SPI Flash; UART for ISP (In System Programming), serial communication, or debugging via Hyper-Terminal.

The NX11FS2x supports C language programming that provides customers with more controllability over complicated projects. Besides, it also brings Q-Code (High-level script programming) to 32-bit MCU that provides customers with an easy-to-use, highly productive development environment for quick realization of product concepts. The NX11FS2x is embedded with On-Chip Debugger, which can provide ICE functionality on the actual production chip. Moreover, it allows for ICP (In-Circuit Programming) to change code / content right on the target board and ISP (In-System Programming) that makes possible on-board re-programming and code/content updates in the system.

Various low-cost package forms are available for the NX11FS2x: SOP-8 / SOP-16 / SSOP-24, to fit in diversified application needs.

2. FEATURES

- Wide Operating Voltage: 2.0V ~ 5.5V
 - Min. operating voltage is 2.0V for max. CPU clock @ 40MHz .
- 32-bit CPU core
 - Andes N705-S, like ARM Cortex-M0+.
 - Max. CPU clock @ 40MHz with 1 wait-state @ EF access.
 - 1-cycle fast multiplier, 7-cycle fast divider.
 - Instruction Local Memory & Data Local Memory employed.
- There are 5 single-die bodies for the NX11FS2x.

P/N	VDD	RAM	EF	Duration (Sec)		I/O	SPI 0	UART	16-bit Timer	PWM -IO	Dual Clock	Cap Touch	DA C	Power Amp.	IR Tx	IR Wakeup	LVD	OCD	Package
				16Kbps	24Kbps														
NX11FS2HA	2.0V ~ 5.5V	4KB	0.5Mb	25	16	4 12	- v	v	2	1 3	v	v	-	Σ-Δ PWM	v	HW	v	-	SOP-8 SOP-16
NX11FS20A	2.0V ~ 5.5V	4KB	1Mb	57	38	4 12	- v	v	2	1 3	v	v	-	Σ-Δ PWM	v	HW	v	-	SOP-8 SOP-16
NX11FS21A	2.0V ~ 5.5V	4KB	2Mb	123	82	4 12	- v	v	2	1 3	v	v	-	Σ-Δ PWM	v	HW	v	-	SOP-8 SOP-16
NX11FS22B	2.0V ~ 5.5V	4KB	4Mb	254	169	4 12 20	- v v	v	2	1 7 8	v	v	-	Σ-Δ PWM	v	HW	v	v	SOP-8 SOP-16 SSOP-24
NX11FS23A	2.0V ~ 5.5V	4KB	8Mb	516	344	4 12 20	- v v	v	2	1 7 8	v	v	14-bit	Σ-Δ PWM	v	FW	v	v	SOP-8 SOP-16 SSOP-24

Table 1 Product Line-Up of NX11FS2x

- Built-in high-reliability 0.5Mb ~ 8Mb Embedded Flash
 - 10 years of data retention
 - 100K times of erase/programming cycles
 - Storage for program code and preset content
- Built-in 4KB RAM
- Built-in oscillators for I_HRC (40MHz) and I_LRC (32,768Hz), accuracy trimmed to +/-1.0% for I_HRC and +/-3.0% for I_LRC.
- Power management to support 3 operating modes per system requirement: Normal / Standby / Halt modes.
At Halt mode, the typical current consumption is 2uA @ 5.5V.
- 8-level LVD (Low Voltage Detection): 3.6V, 3.4V, 3.2V, 3.0V, 2.8V, 2.4V, 2.2V, 2.0V. Reference voltage 3.4V trimmed to +/-3% accuracy before shipping.
- Built-in LVR (Low Voltage Reset) function.
- Two Timers (Timer0 / Timer1), each Timer consists of a 16-bit down-counter with various clock sources.
- Built-in 14-bit resolution DAC output for driving speaker via external power amplifier (only for NX11FS23A)
- Built-in 13-bit Σ-Δ PWM power amplifier to drive speaker directly
- Up to 20 pins of GPIO
 - Bit configurable for every I/O pin by register control, except byte-defined strength of pull-up resistors
 - Multi-function pins via register control

- SPI Flash interface supported @ SPI0
 - Master mode, up to 32MHz clock speed
 - 32-bit mode supported to address beyond 128Mb
 - Support Data mode and XIP mode (eXecute In Place)
 - Support Single / Dual / Quad I/O modes of SPI Flash
- IR TX supported (via Timer 0 / 1)
- RTC with optional 16.384KHz / 1.024KHz / 64Hz / 2Hz interrupts
- WDT (Watch-Dog Timer) supported with optional 188ms / 750ms reset periods
- ISP (In-System Programming) supported
 - Source: UART
 - Destination: EF, SPI Flash (via program control)
 - ISP boot code protected from accidental erasure
- UART H/W supported
 - Full-duplex TX/RX with 1-level FIFO
 - Baud rates @ 115,200 / 230,400 / 460,800 / 1Mbps
- Up to two PWM-IO Generators
 - Each generator with 4 PWM-IO pins (PWMA0 ~ PWMA3 / PWMB0 ~ PWMB3)
 - Each generator got one 16-bit timer, which could be used as a general timer
 - Independent 16-bit duty cycle register per PWM-IO pin
 - NX11FS2HA / NX11FS20A / NX11FS21A got only one set of PWM-IO generator (PWMA)
- CapTouch sensor supported
 - All pins of PA port are optional as CapTouch sensing pads
- Support EF Security Lock mechanism to prevent programmed data from being read out
- Easy-to-use Development Environment
 - High-level Q-Code programming supported
 - Advanced C-Module programming supported
 - 2-pin OCD (On-Chip Debugger) supported with source-level debugging for both Q-Code and C-Module
(Not available @ NX11FS2HA / NX11FS20A / NX11FS21A)
 - Multi-purpose NX_Programmer for ICE debugging and programming of EF / SPI Flash
 - Smart Writer used in MP for EF/SPI Flash pre-programming @ packages, or ICP @ target boards
 - 6-pin programming interface (VDD, VSS, PD0, PD1, PA12, RSTB/PA8) supported
- S/W-based Speech/MIDI decoder & various algorithms supported
 - ADPCM Decoder (Adaptive Differential PCM): 4 channels, 4-bit / 5-bit per sample
 - SBC Decoder (Sub-Band Coding): 1 channel, 4.5K ~ 32Kbps, max. 16KHz bandwidth

- MIDI: up to 8-channel polyphonic melody @ 32KHz Output Sample Rate
- Playback Voice Effects: speed change with pitch fixed, pitch change with speed fixed, etc.
- Noise filter @ 4x/8x/16x/32x up-sampling supported
- Shipping Form
 - Single-Die Package: SOP-8 / SOP-16 / SSOP-24

3. BLOCK DIAGRAM

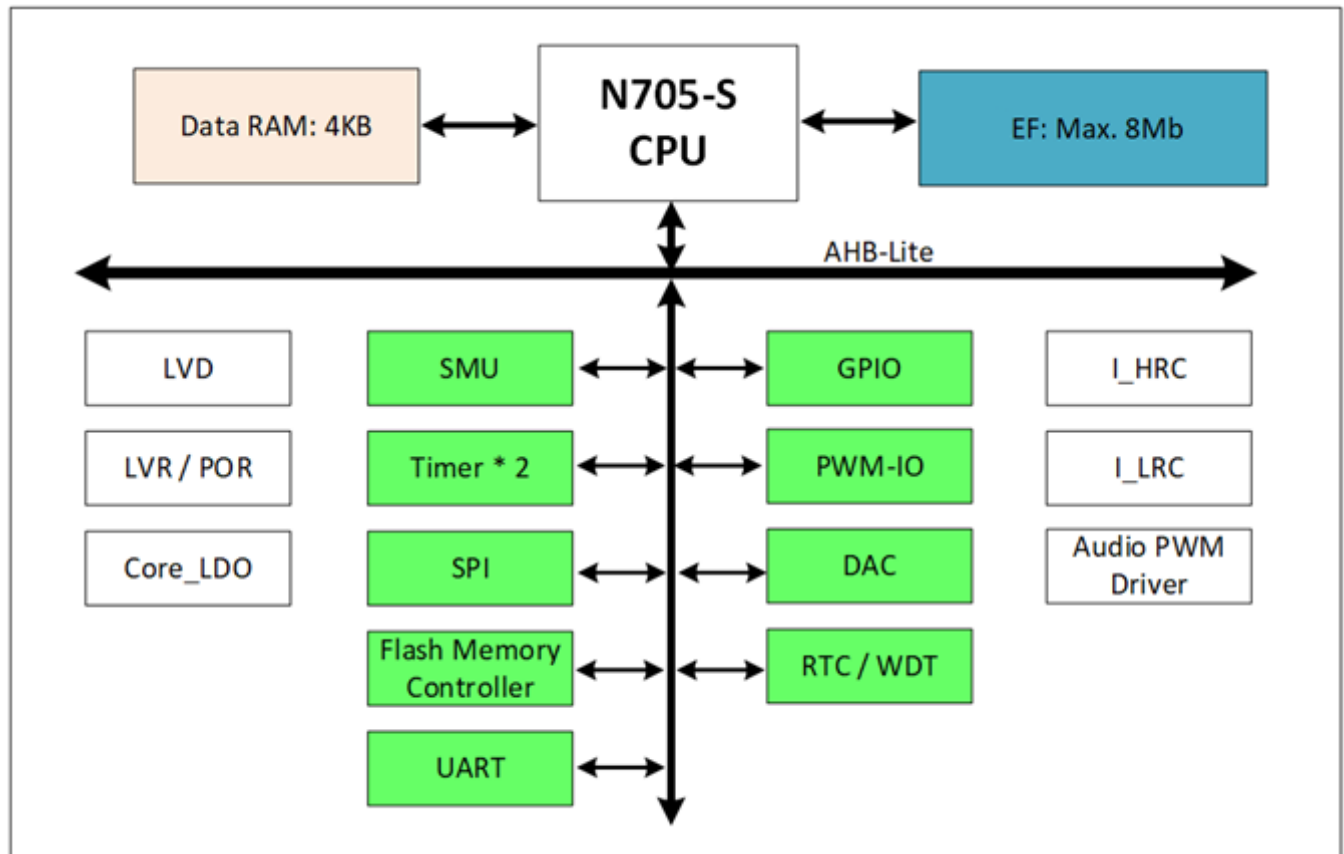


Figure 1 Block Diagram of NX11FS2x Series

4. PAD / PIN DESCRIPTION

Pad Name	Alt #	Type	SOP-8	SOP-16	SSOP-24	Pad Description
Part No.	-	-	NX11FS2xAS8 NX11FS22BS8	NX11FS2xAS16 NX11FS22BS16	NX11FS22BU24 NX11FS23AU24	-
Power						
VDD	0	P	•	•	•	Power input
VDD_PWM	0	P				Power for DAC and audio PWM driver. Connected to VDD internally, if not available separately.
VSS	0	P	•	•	•	Ground
VSS_PWM	0	P				Ground for DAC and audio PWM driver. Connected to VSS internally.
PWM / DAC						
PWM1 / DAC	0	O	•	•	•	Audio PWM driver output 1 or DAC output by option
PWM2	0	O	•	•	•	Audio PWM PA output 2
Port A						
PA1	0	I/O			•	GPIO pin PA1
IR0	1	O			•	IR Tx output from Timer0
PA2	0	I/O		•	•	GPIO pin PA2
IR1	1	O		•	•	IR Tx output from Timer1
INT0	2	I		•	•	External INT0
PA3	0	I/O		•	•	GPIO pin PA3
TM0	1	I		•	•	External input for Timer0 / Timer1
INT1	2	I		•	•	External INT1
PA4	0	I/O			•	GPIO pin PA4
PA5	0	I/O			•	GPIO pin PA5
PA6	0	I/O			•	GPIO pin PA6
TX	1	O			•	TX pin of UART
PA7	0	I/O			•	GPIO pin PA7
RX	1	I			•	RX pin of UART
RSTB/PA8	0	I, I/O	•	•	•	RSTB (default) or GPIO pin by option. Since this pin is RSTB by default upon power up, so that it can't be set at low level when powered on.
BCSB	3	I	•	•	•	Programming I/F
PA12	0	I/O	•	•	•	GPIO pin PA12
PWMA0	1	O	•	•	•	PWMA0 output pin
BMISO	3	O	•	•	•	Programming I/F
PA13	0	I/O		•	•	GPIO pin PA13
PWMA1	1	O		•	•	PWMA1 output pin
PA14	0	I/O		•	•	GPIO pin PA14
PWMA2	1	O		•	•	PWMA2 output pin
PA15	0	I/O			•	GPIO pin PA15
PWMA3	1	O			•	PWMA3 output pin

Pad Name	Alt #	Type	SOP-8	SOP-16	SSOP-24	Pad Description
Part No.	-	-	NX11FS2xAS8 NX11FS22BS8	NX11FS2xAS16 NX11FS22BS16	NX11FS22BU24 NX11FS23AU24	-
Port B						
PB0	0	I/O		•	•	GPIO pin PB0
PWMB0	1	O		•	•	PWMB0 output pin (only for NX11FS22B / NX11FS23A)
SPI0_IO1	2	O		•	•	IO1 / MISO pin of SPI0
PB1	0	I/O		•	•	GPIO pin PB1
PWMB1	1	O		•	•	PWMB1 output pin (only for NX11FS22B / NX11FS23A)
SPI0_CSB	2	O		•	•	CSB pin of SPI0
PB2	0	I/O		•	•	GPIO pin PB2
PWMB2	1	O		•	•	PWMB2 output pin (only for NX11FS22B / NX11FS23A)
SPI0_CLK	2	O		•	•	CLK pin of SPI0
PB3	0	I/O		•	•	GPIO pin PB3
PWMB3	1	O		•	•	PWMB3 output pin (only for NX11FS22B / NX11FS23A)
SPI0_IO0	2	I/O		•	•	IO0 / MOSI pin of SPI0
PB4	0	I/O			•	GPIO pin PB4
SPI0_IO2	2	I/O			•	IO2 pin of SPI0
PB5	0	I/O			•	GPIO pin PB5
SPI0_IO3	2	I/O			•	IO3 pin of SPI0
Port D						
PD0	0	I/O	•	•	•	GPIO pin PI0
ICE_CLK	1	O	•	•	•	Clock pin of ICE port
TX	2	O	•	•	•	TX pin of UART
TSCL	3	I	•	•	•	Programming I/F
PD1	0	I/O	•	•	•	GPIO pin PI1
ICE_DAT	1	I/O	•	•	•	Data pin of ICE port
RX	2	I	•	•	•	RX pin of UART
TSDA	3	I/O	•	•	•	Programming I/F

Pad Type: P = Digital Power, I = Input, O = Output, I/O = Input / Output, AI = Analog Input, AO = Analog output, AP = Analog Power.

5. FUNCTIONAL DESCRIPTION

5.1 Memory Organization

The memory map is depicted in Figure 2 Memory Map of the NX11FS2x Series. The Embedded Flash, RAM, function registers, and interrupt vectors, are all memory mapped. The embedded flash size ranges from 64KB @ NX11FS2HA up to 1MB @ NX11FS23A, including interrupt vectors, AP code and various kinds of data. There are 4KB of Data RAM associated with the N705-S processor for running the program @ EF / SPI Flash.

Total addressing space is 16MB, while SPI Flash is mapped within 0x80_0000 ~ 0x9F_FFFF (2MB space) with bank support for XIP and data storage expansion.

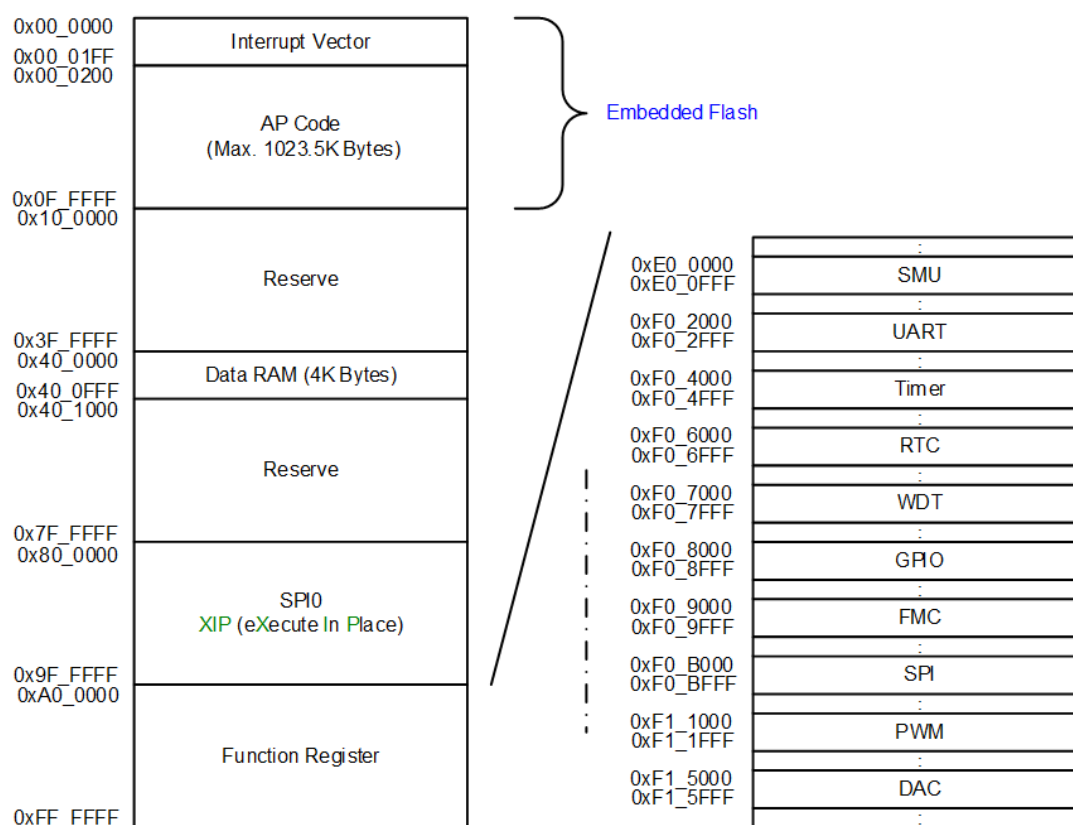


Figure 2 Memory Map of the NX11FS2x Series

5.2 Clock Generator

The clock generator consists of 2 clock sources:

- Built-in high clock (I_HRC): Output frequency is 40MHz with 1 wait-state @ EF access.
- Built-in low clock (I_LRC): Output frequency is 32,768Hz.

These two internal oscillators, I_HRC and I_LRC, are trimmed to achieve +/-1.0% and +/-3% accuracy, respectively.

5.3 Operating Mode

The NX11FS2x provides three kinds of operating modes to tailor for various kinds of applications while saving power consumption. These operating modes are normal mode, standby mode and halt mode.

Normal mode is designated for high-speed, high-performance operation. At standby mode, the NX11FS2x stops almost all operations, except peripheral blocks with clock source from I_LRC, and wake-up periodically to serve scheduled routines. At halt mode, it stops all operations, waiting for external events to wake it up.

When the NX11FS2x is powered up, there is a delay of 32mS before user's code is executed to ensure proper operation.

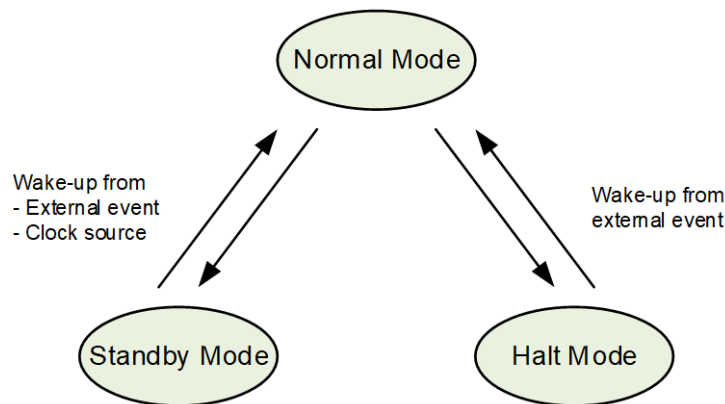


Figure 3 Operating Modes

5.4 Interrupt

Interrupt signals are directly connected to the N705-S processor. The interrupt priority is controlled by the processor. Each interrupt is assigned with 2 bits to represent 4 possible priority levels ranging from 0 (highest) to 3 (lowest). The hardware compares the priority level first: the smaller the priority level, the higher the priority. With the same priority, the lower the interrupt number, the higher the priority.

5.5 Peripherals

5.5.1 I/O Port

Up to 20 GPIO pins are available. These are shared multiple function pins under control of the alternate multiple function registers. A total of 20 pins are arranged in 3 ports named with Port A (PA), Port B (PB), and Port D (PD). The PA port has 12 pins, PB port 6 pins, and PD port 2 pins.

Each pin can be configured as input or output, weak / strong pull-high resistor and can wake up CPU upon I/O state changes from halt mode.

5.5.2 SPI

There is one SPI master supported @ SPI0 that is dedicated for connecting with an external SPI Flash device to store the data used for various applications like speech (ADPCM, SBC), melody (including MIDI file and wavetable timbres), and user's general data storage. With single/dual I/O modes supported, the SPI Flash can run up to 20MHz clock. Together with the XIP capability (eXecute In Place), users can extend the program code @ EF to the SPI Flash with a descent performance for many applications.

There is no dedicated LDO inside NX11FS2x to power the SPI Flash. Users have to take care of the power supply, either via external LDO or voltage drop of VDD, depending on the battery condition.

5.5.3 UART

The NX11FS2x provides the UART (Universal Asynchronous Receiver Transmitter) module, which is a full-duplex, asynchronous communication channel that communicates with peripheral devices and personal computers through protocols such as RS-232.

- Support 5 to 8 bits per character
- Support 1, 1.5 and 2 STOP bits
- Support even, odd and stick parity bits
- Support programmable baud rate
- Support detection of parity error, framing error and data overrun

5.5.4 PWM-IO

The NX11FS2x has up to 2 sets of PWM-IO generators (PWMA / PWMB), each with four PWM-IO outputs (PWMA0 ~ PWMA3, PWMB0 ~ PWMB3). Every four PWM-IO output pins share a common 16-bit PWM-IO timer, while each PWM-IO output pin has its own duty register. Be noted that NX11FS2HA / NX11FS20A / NX11FS21A got only 3 pins of PWMA available.

- Four PWM-IO outputs share a 16-bit timer
- Programmable divider as the clock source of timer
- 16 bits for PWM's duty cycle

5.6 Timer

The NX11FS2x has two 16-bit timers: TIMER0 / TIMER1, which can be used as a trigger source for DAC / Audio PWM / IR / Software CapTouch or as a function of time delay, clock generation, etc.

- Programmable source of timer clock
- 16-bit counter for each timer

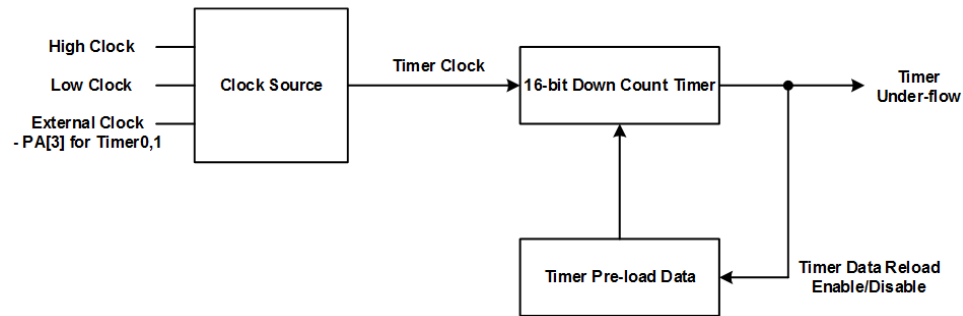


Figure 4 Timer Block Diagram

5.7 Software CapTouch

The NX11FS2x supports S/W-based CapTouch on all PA pins for applications that require no very low standby current with wake-up on CapTouch feature. The power consumption of S/W-based CapTouch might not be low enough to meet the strict battery life criterion, but it's still useful for many applications since the BOM cost is virtually not changed at all after the inclusion of CapTouch feature.

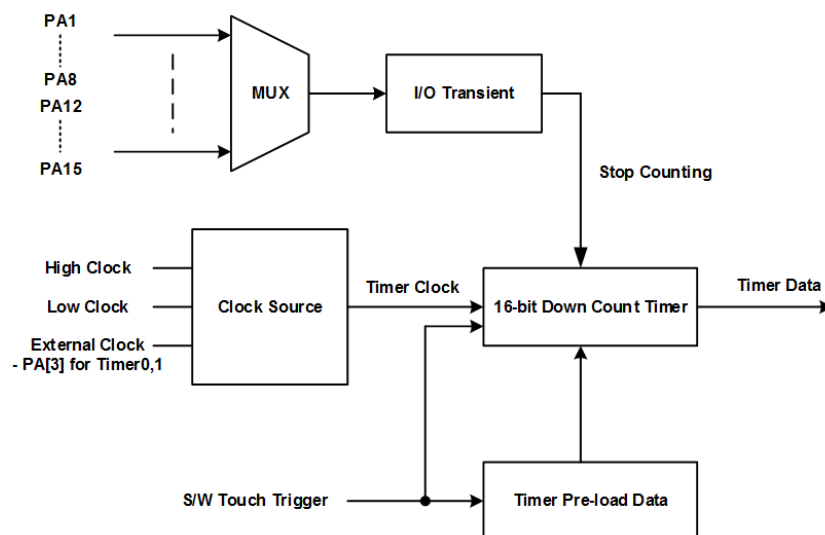


Figure 5 Software CapTouch Block Diagram

5.8 IR TX

The NX11FS2x provides a programmable IR carrier, whose frequency can be generated by assigning suitable counter values to the 16-bit timer.

- Support output stop value at 0 or 1.
- Support 16 bits reload data to adjust IR's frequency.
- The lowest frequency is I_HRC divided by 65535, which is 512 Hz @ I_HRC=40MHz .

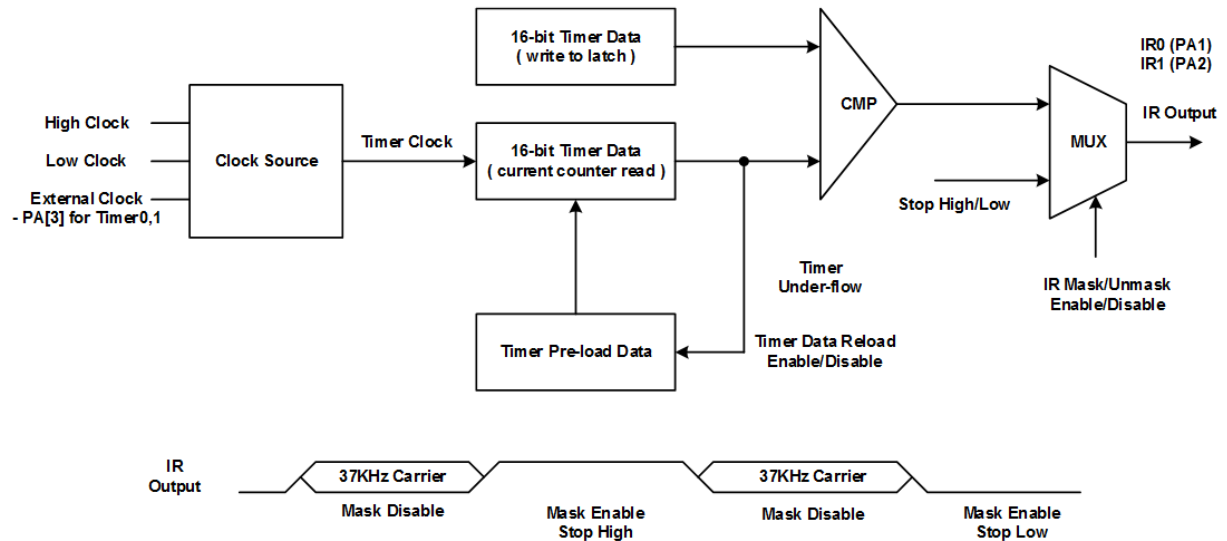


Figure 6 IR TX Block Diagram

5.9 RTC

As the name implies, the RTC (Real-Time Clock) is generally used to keep the time, with the clock source from an internal built-in I_LRC (trimmed to 32,768Hz with +/-1.5% accuracy). The RTC supports periodic time tick interrupts with 4 options: 16.384KHz, 1.024KHz, 64Hz, 2Hz.

5.10 WDT

The Watchdog Timer (WDT) is used to perform a system reset when the system is not responding at all. There are two period options for the WDT to generate a reset: 188ms / 750ms.

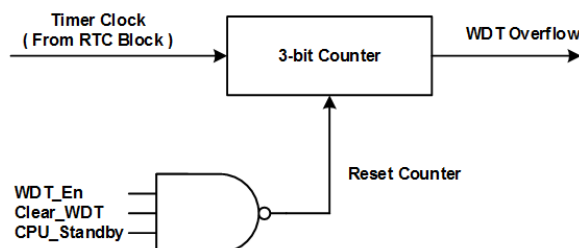


Figure 7 WDT Block Diagram

5.11 DAC & Audio PWM Driver

The NX11FS2x provides one data buffer with 1-level FIFO and one 14-bit Digital-to-Analog converter (for NX11FS23A only) with interpolation function. It can be started by software or TIMER trigger.

- Provide 1-level FIFO as data buffer
- Provide hardware up-sampling (interpolation) function

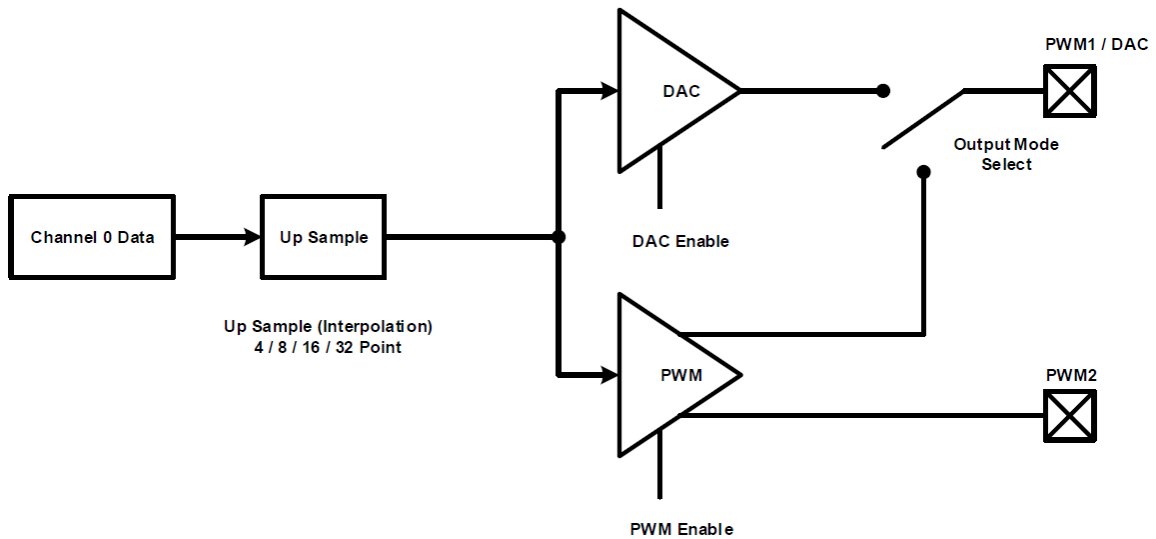


Figure 8 Block Diagram of DAC and Audio PWM Driver

5.12 LVD

The LVD (Low Voltage Detector) is trimmed to +/-3% accuracy for the user to detect the battery voltage @ VDD pin. When the VDD voltage falls below the specified LVD level, the LVD_Flag will be set as HIGH.

LVD_SEL[2:0]	Voltage
111	3.6V
110	3.4V
101	3.2V
100	3.0V
011	2.8V
010	2.4V
001	2.2V
000	2.0V

Table 2 LVD voltage select

5.13 Options

Users may select different options depending on the application requirement. There are several options that users may select for the NX11FS2x series, as shown in Table 3 User Options.

Item	Name	Options
1	Reset Pin (PA8)	1. Reset Pin (default) 2. GPIO
2	LVR (Halt Mode)	1. LVR Enable at Halt Mode 2. LVR Disable at Halt Mode (default)
3	VDD Voltage	1. 4.5V (default) 2. 3.0V
4	WDT	1. WDT Enable (default) 2. WDT Disable
5	Input Voltage (V_{IH}/V_{IL})	1. 0.7VDD/0.3VDD (CMOS, default) 2. 0.5VDD/0.2VDD (TTL)
6	SPI0 Functions	1. GPIO (default) 2. SPI
7	Voice Output	1. PWM (default) 2. DAC
8	Audio PWM Current	1. Normal (default) 2. Large 3. Ultra

Table 3 User Options

6. ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Rating

Symbol	Parameter	Rated Value	Unit
$V_{DD} - V_{SS}$	Supply voltage	-0.5 ~ +7.5	V
V_{IN}	Input voltage	$V_{SS} - 0.3 \sim V_{DD} + 0.3$	V
T_{OP}	Operating Temperature	0 ~ +70	°C
T_{ST}	Storage Temperature	-25 ~ +85	°C

6.2 DC Characteristics

($T_A=25^{\circ}\text{C}$, unless otherwise specified)

Symbol	Parameter		V _{DD}	Min.	Typ.	Max.	Unit	Condition
V _{DD}	Operating voltage		-	2.0		5.5	V	-
I _{HALT}	Halt Current		5.5		2		uA	CPU stops, all functions off
			5.5		3		uA	LVR on at halt mode
I _{SB}	Standby Current ⁴		3		3		uA	CPU stops, all functions off, RTC on, LVR on
			4.5		4			
I _{OP}	Operating Current	Normal Mode	3		7		mA	CPU_CLK = 40MHz , 1 wait-state, No load
			4.5		7			
R _{PH}	Pull High Resistor (Input current)	Strong (100KΩ)	3		100		KΩ	V _{IN} = 0V
			4.5		66			
		Weak (1MΩ)	3		1,000			
			4.5		600			
		RSTB (30KΩ)	3		30			
			4.5		20			
I _{OH}	Normal drive current (Normal GPIO)		3		-9		mA	V _{OH} = V _{DD} - 1.0V
			4.5		-13			
	SPI mode drive current (SPI0 PB[0:5])		3		-14			V _{OH} = V _{DD} - 1.0V, SPI mode
			4.5		-20			
I _{OL}	Normal sink current (Normal GPIO)		3		12		mA	V _{OL} = 1.0V
			4.5		19			
	Large sink current		3		23			

Symbol	Parameter	V _{DD}	Min.	Typ.	Max.	Unit	Condition
	(Normal GPIO ¹)	4.5		36			V _{OL} = 1.0V, SPI mode
	SPI mode sink current (SPI0 PB[0:5])	3		14			
		4.5		20			
I _{PWM}	Audio PWM Output Current ²	3		150		mA	1KHz Sine wave, THD+N @ 1%, Load = 8Ω
		4.5		250			
ΔF/F	I_HRC trim accuracy	3	-0.5		0.5	%	$\frac{F_{osc} - F_{typ}^3}{F_{typ}}$
V _{LVR}	LVR voltage	-		1.8		V	V _{LVR} is trimmed to 1.8V +/- 0.1V.

^{*1} PB4 sink capability is rated at 15mA / 23mA for 3V / 4.5V, respectively.

^{*2} The current is represented in the form of effective power, which is bigger than playback under practical conditions.

^{*3} F_{typ} = 40MHz, which is the nominal clock of I_HRC.

^{*4} I_{SB} (Standby Current) is specially designed for NX11FS2HA / NX11FS20A / NX11FS21A / NX11FS22B to meet the battery life challenge of IR wake-up applications. It can reach 5uA sleep current @ 500mS scan period, 4.5V condition.

6.3 DAC Characteristics

($V_{DD}=4.5V$, $T_A=25^{\circ}C$, unless otherwise specified)

Symbol	Characteristics	Min.	Typ.	Max.	Unit	Condition
B _{RES}	Resolution of DAC			14	Bit	-
THD+N	THD+N ($V_{in} = -3$ dBFS)		-66		dBr A	No load
DR	Dynamic Range ($V_{in} = -60$ dBFS)		-77		dBr A	
SNR	Noise at No Signal ($V_{in} = -90$ dBFS)		-100		dBr A	

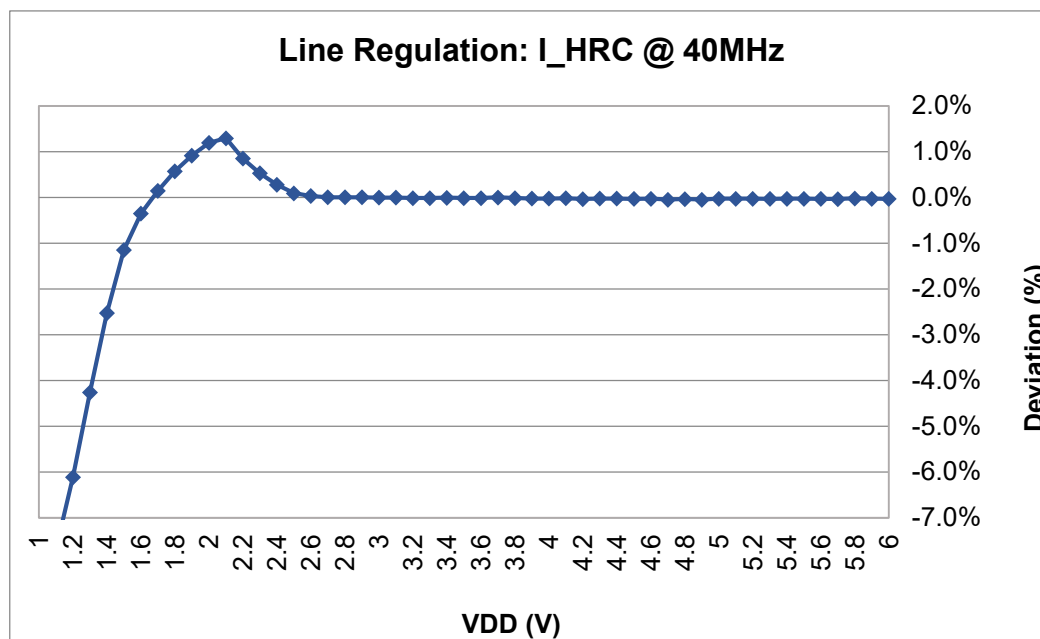
6.4 Audio PWM Characteristics

($V_{DD}=4.5V$, $T_A=25^{\circ}C$, unless otherwise specified)

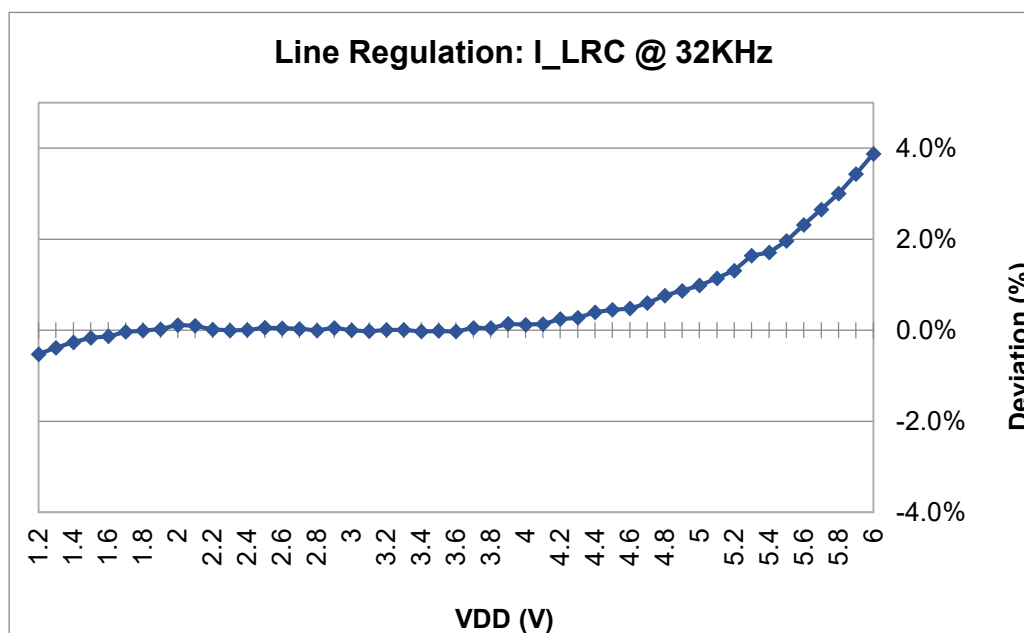
Symbol	Characteristics	VDD	Min.	Typ.	Max.	Unit	Condition
THD+N	THD+N ($V_{in} = -3$ dBFS)	-		-60		dBr A	Load = 8Ω
DR	Dynamic Range ($V_{in} = -60$ dBFS)	-		-81		dBr A	
SNR	Noise at No Signal ($V_{in} = -90$ dBFS)	-		-125		dBr A	
P _o	Output Power	3V		230		mW	Load = 8Ω, THD+N @ 1%
		4.5V		530		mW	Load = 8Ω, THD+N @ 1%

6.5 Frequency vs. Voltage

6.5.1 I_HRC

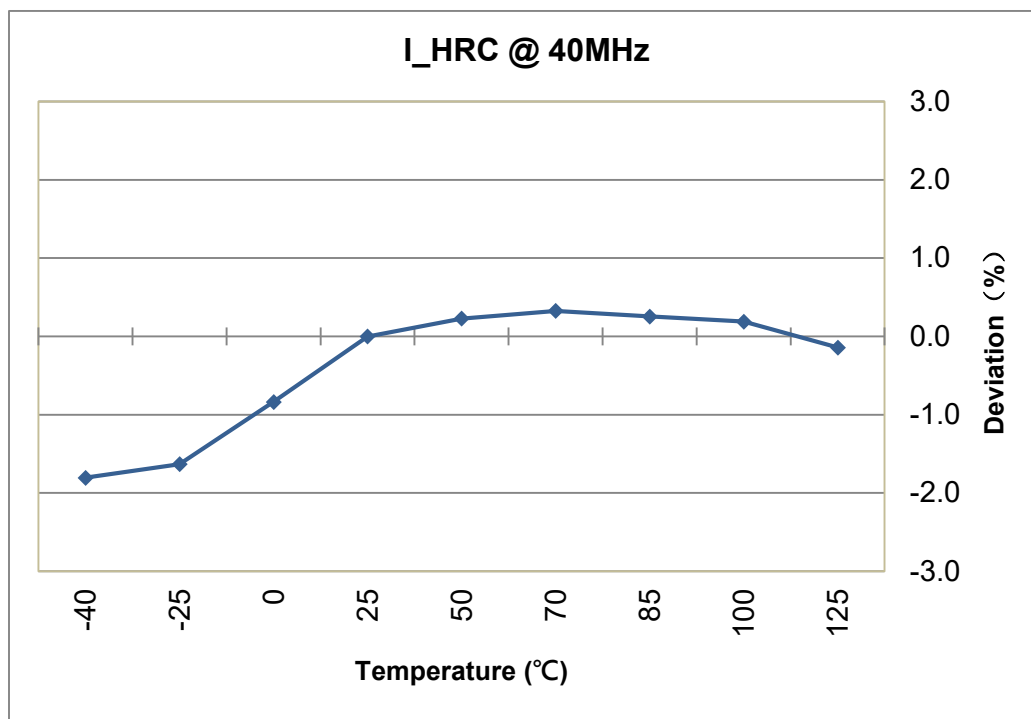


6.5.2 I_LRC

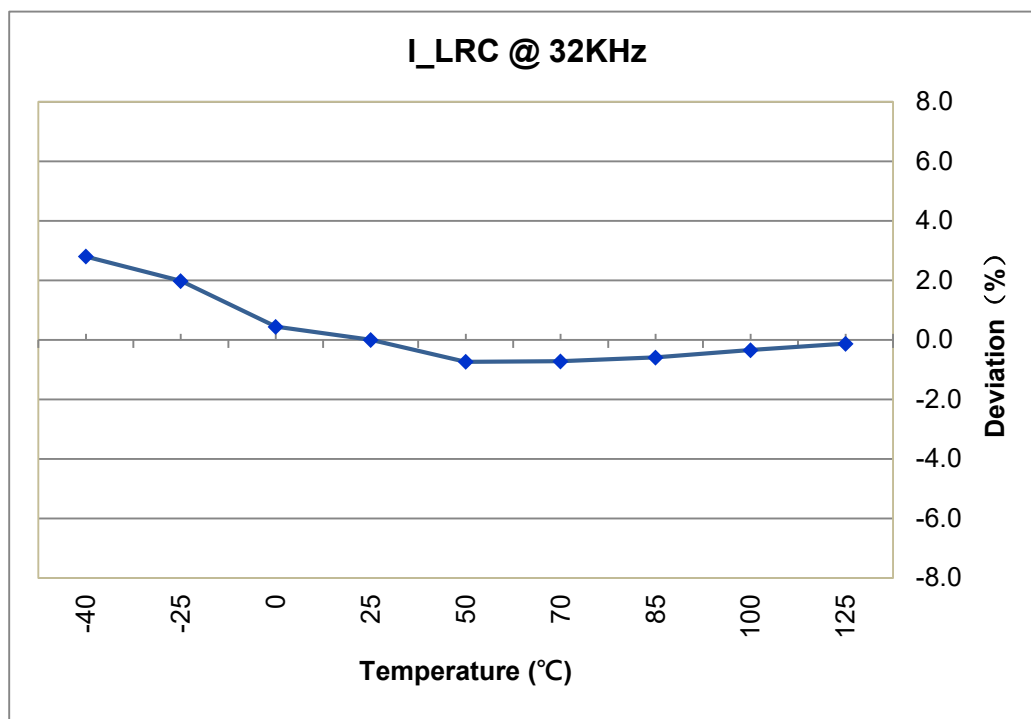


6.6 Frequency vs. Temperature

6.6.1 I_HRC

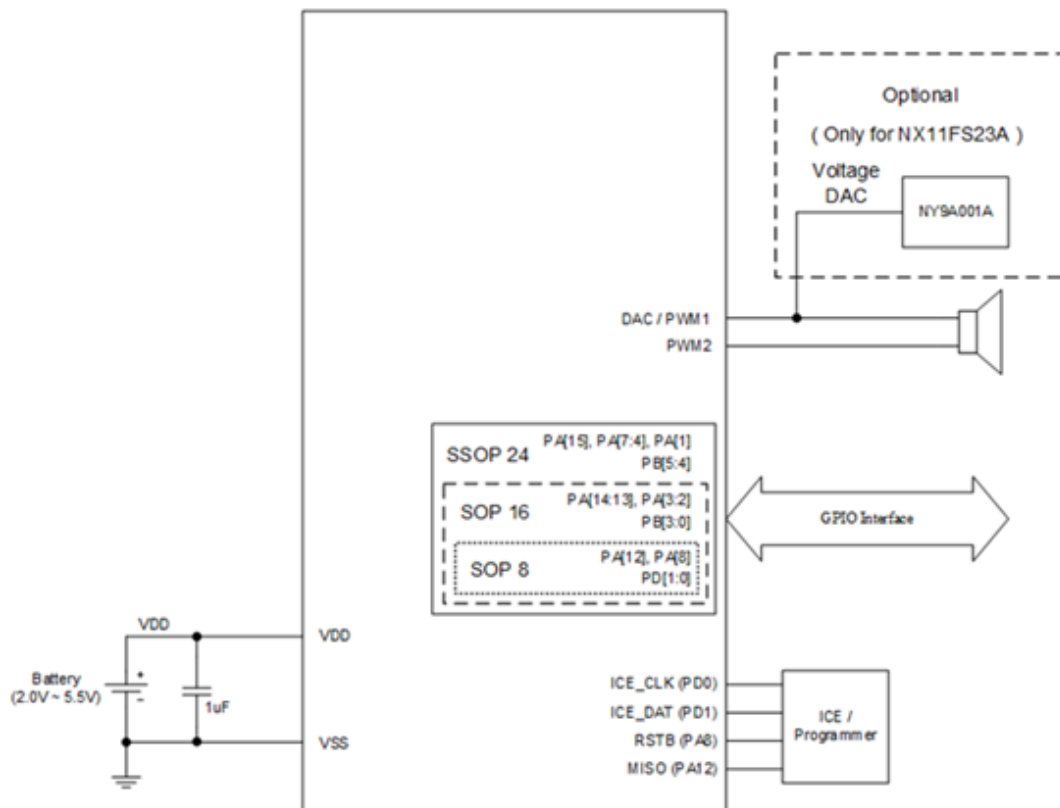


6.6.2 I_LRC



7. APPLICATION CIRCUIT

- NX11FS2xA/B



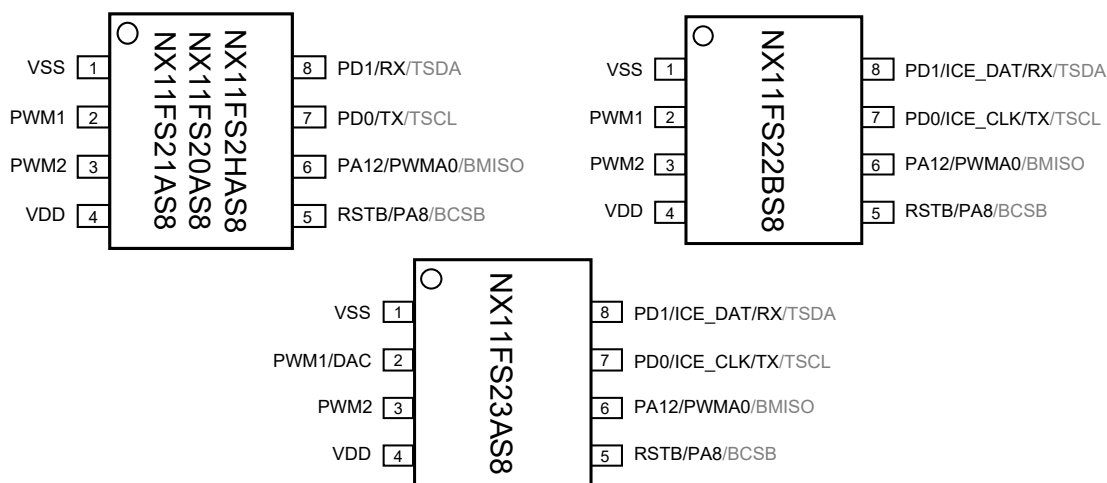
*Note 1: NX11FS23A_EVB can pass FCC Part 15B test, under the condition of 3*Alkaline batteries, 40MHz @ I_HRC, 20MHz SPI clock, playback of SBC from SPI Flash, 8-ohm speaker, and LED toggle on/off @ 2Hz.*

Note 2: The 1uF decoupling capacitor @ VDD/VSS is required and should be placed as close to the chip as possible.

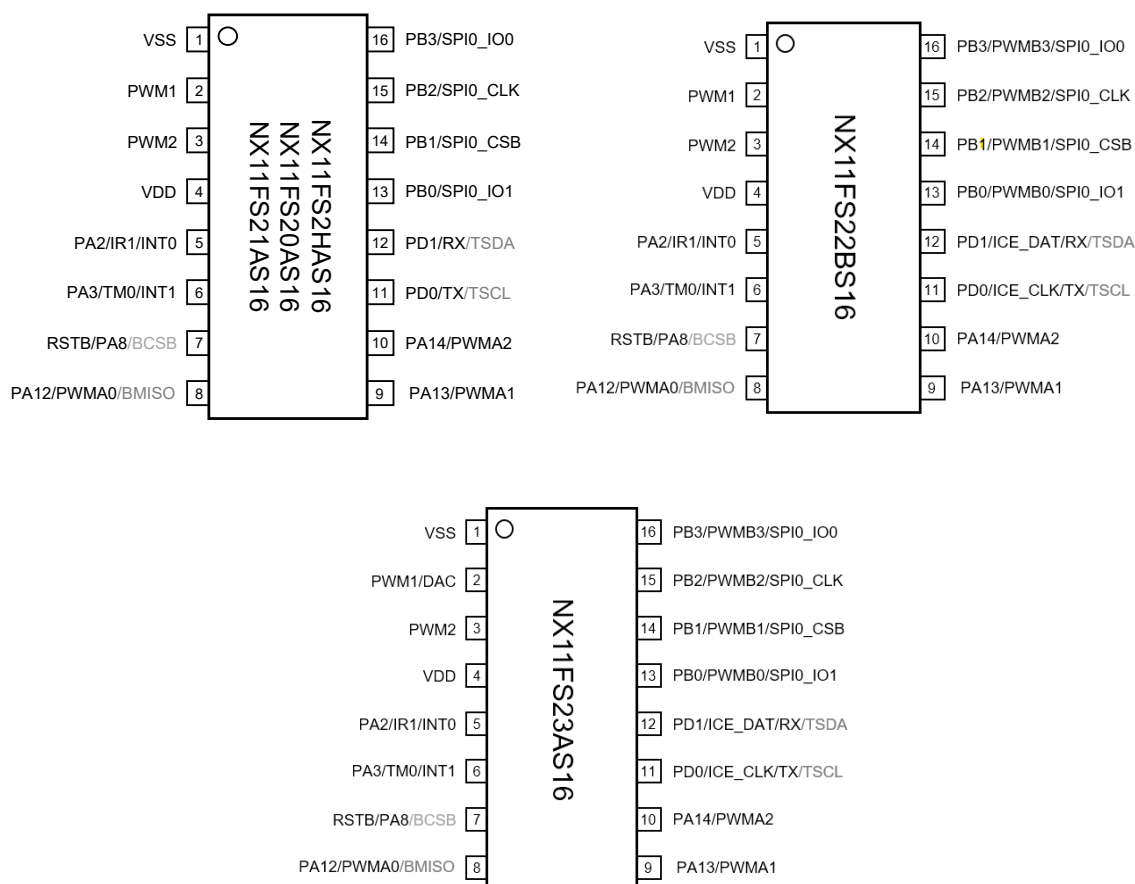
Note 3: Do not add small cap (like 0.1uF) across trigger switches in parallel to avoid negative pulses.

8. PACKAGE PIN ASSIGNMENT

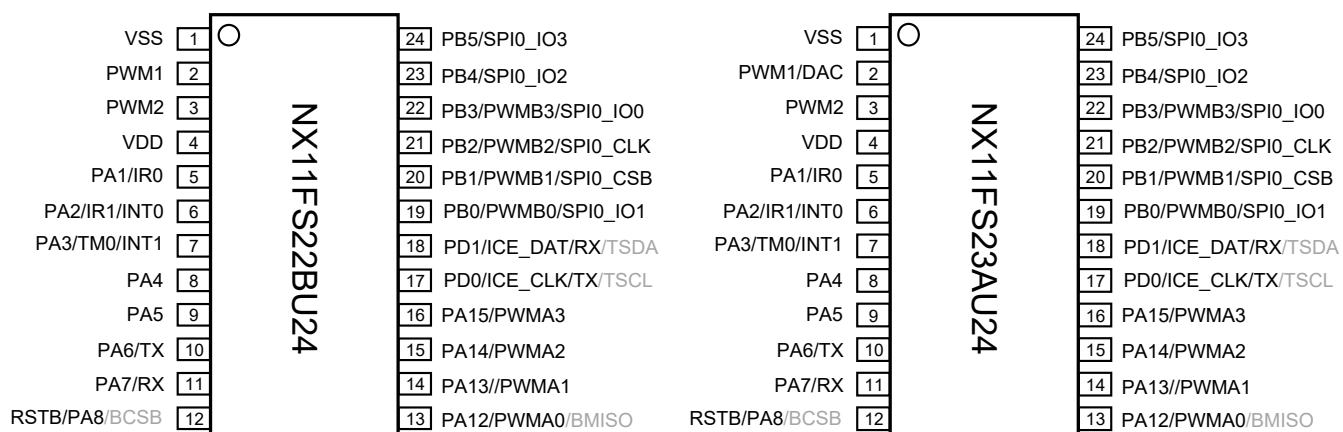
8.1 SOP-8 (150mil, 1.27mm pin pitch)



8.2 SOP-16 (150mil, 1.27mm pin pitch)

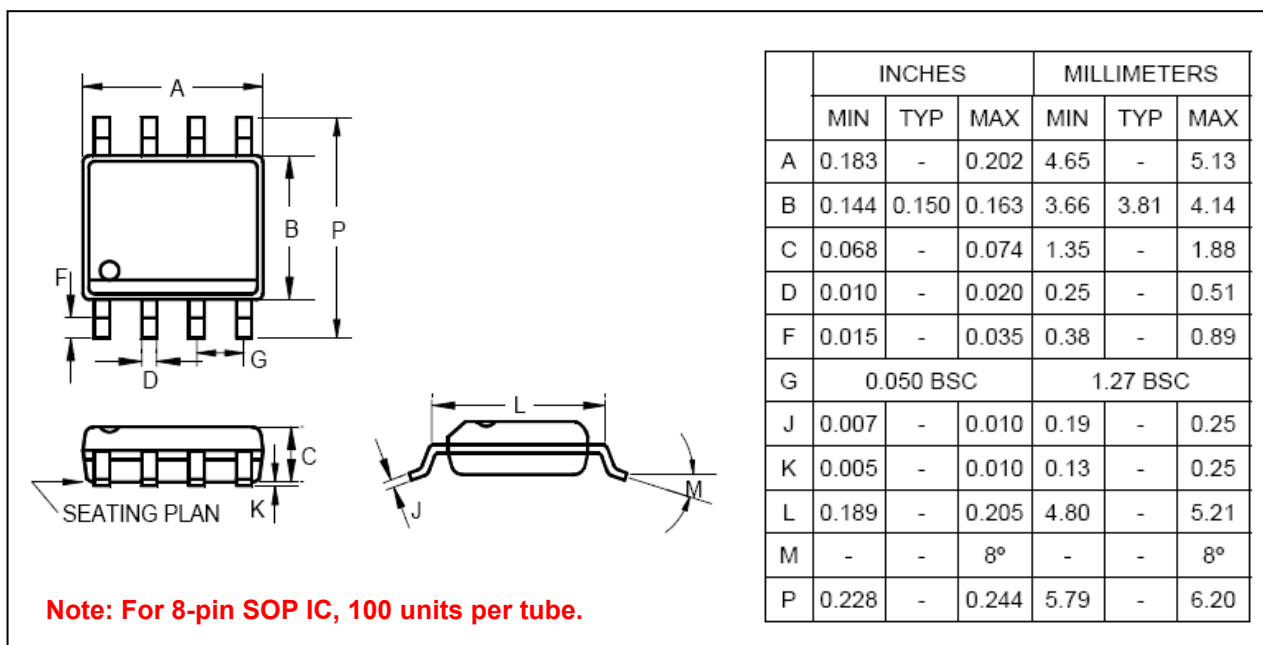


8.3 SSOP-24 (150mil, 0.635mm pin pitch)

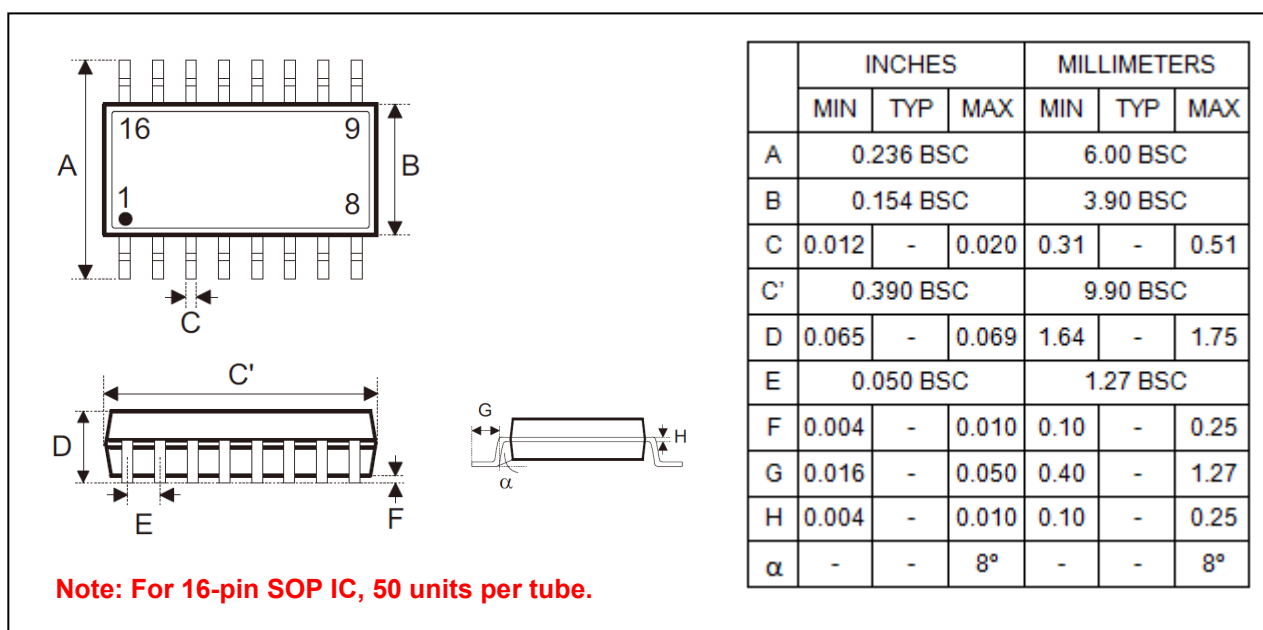


9. PACKAGE DIMENSION

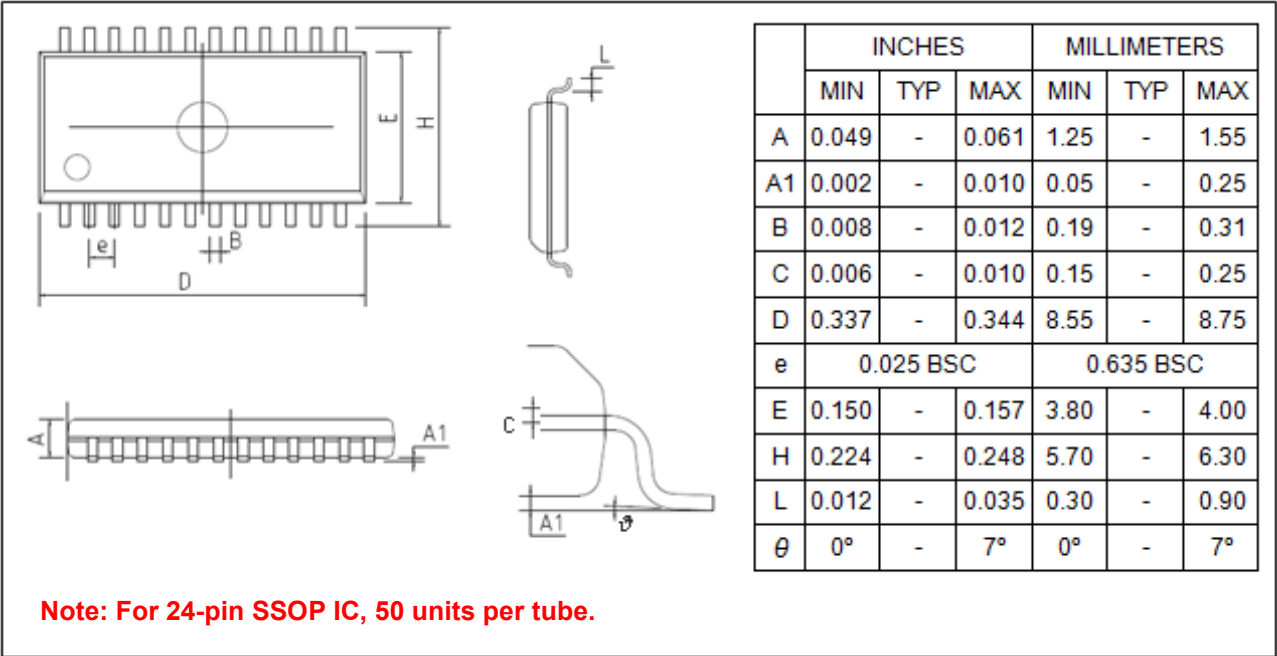
9.1 SOP-8 (150mil, 1.27mm pin pitch)



9.2 SOP-16 (150mil, 1.27mm pin pitch)



9.3 SSOP-24 (150mil, 0.635mm pin pitch)



10. ORDERING INFORMATION

<i>P/N</i>	<i>Shipping Form</i>	<i>Remark</i>
NX11FS2HAW	Wafer	Blank EF data
NX11FS2HAS8	SOP-8	150 mil, 1.27mm pitch
NX11FS2HAS16	SOP-16	150 mil, 1.27mm pitch
NX11FS20AW	Wafer	Blank EF data
NX11FS20AS8	SOP-8	150 mil, 1.27mm pitch
NX11FS20AS16	SOP-16	150 mil, 1.27mm pitch
NX11FS21AW	Wafer	Blank EF data
NX11FS21AS8	SOP-8	150 mil, 1.27mm pitch
NX11FS21AS16	SOP-16	150 mil, 1.27mm pitch
NX11FS22BW	Wafer	Blank EF data
NX11FS22BS8	SOP-8	150 mil, 1.27mm pitch
NX11FS22BS16	SOP-16	150 mil, 1.27mm pitch
NX11FS22BU24	SSOP-24	150 mil, 0.635mm pitch
NX11FS23AW	Wafer	Blank EF data
NX11FS23AS8	SOP-8	150 mil, 1.27mm pitch
NX11FS23AS16	SOP-16	150 mil, 1.27mm pitch
NX11FS23AU24	SSOP-24	150 mil, 0.635mm pitch